A New Leakage-Tolerant Design for High Fan-in Domino Circuits

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Abstract

In this paper, a new leakage-tolerant circuit design technique for high fan-in domino circuits is presented. This technique uses stacking effect to reduce the leakage of the evaluation network of domino gates. It also uses a current mirror in parallel with the evaluation network to reduce the evaluation delay. Depending on the fain-in, the proposed technique exhibits 2.0X to 17.7X leakage and noise tolerance improvement compared to a standard domino counterparts designed in a 70-nm technology node.

Keywords: Domino, High fan-in, Leakage-tolerant, Noise immunity, Power, Technology scaling

I. Introduction

Dynamic logic has been widely used for very high performance that cannot be achieved with the static logic styles [1]. However, the dynamic logic styles are more sensitive to noise than the static logic styles. The poor noise immunity of domino circuits is due to their low switching threshold voltage, which is equals to the threshold voltage of NMOS devices in their evaluation networks. As the technology scales down, the supply voltage is reduced for low power; however, this requires the threshold voltage (V_{th}) scaling to achieve high performance. Threshold voltage reduction results in less noise immunity for domino logic gates. Moreover, reduced threshold voltage exponentially increases subthreshold leakage, as illustrated in Fig. 1. Besides leakage increase, the input noise sources such as crosstalk and supply noise also increase with technology scaling [2]. Due to all of these trends, domino logic circuits suffer from leakage and noise immunity in deep submicron regimes. The leakage immunity is more problematic in high fan-in domino circuits because of larger leakage due to more parallel evaluation paths. Since the leakage current is proportional to fan-in of domino OR-gates, the noise immunity decreases with fan-in increase. Leakage and noise-tolerance are major issues for wide domino OR gates, because the evaluation transistors are all in parallel, leaking the charge from the precharge node [3].

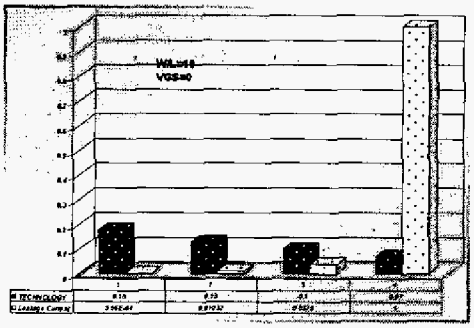

Fig. 1. leakage current and technology scaling

To reduce leakage power while maintaining system performance, dual-V_{th} designs were proposed [4], [5]. The dual V_{th} techniques utilize high V_{th} off the circuit critical paths to reduce leakage current while utilizing low V_{th} on the critical paths to obtain high performance. High V_{th} cannot be used to improve leakage/noise immunity of domino circuits, because domino circuits are used in critical paths of a design to achieve high performance. Moreover, the Dual V_{th} requires an expensive process technology. We propose a new circuit technique for domino logic design that improves leakage immunity of high fan-in domino logic gates without using dual V_{th}.

Fig. 2 shows the conventional standard domino circuits for high fan-in OR gates. The scheme in Fig. 2(a) is a footed standard domino (SD) logic, whereas the one in Fig. 2(b) is a footless standard domino logic. The footed structure typically shows better noise and leakage tolerance because of the leakage reduction in the evaluation path as a result of stacking effect [6]. In the conventional domino circuits (Fig. 2(a),(b)), the robustness of standard domino circuits can be improved by upsizing the keeper transistor [3],[7]. The keeper ratio (K) is defined as the ratio of the current drivability of the keeper transistor to that of the evaluation transistor:

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{keeper transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{evaluation transistor}}} \qquad (1)$$

where μ_n and μ_p are electron and hole motilities, respectively. However, there are limitations on keeper upsizing because of increased current contention between the keeper transistor and the

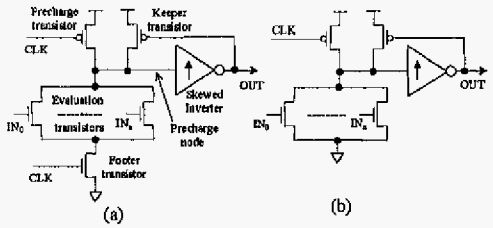

Fig. 2. Standard high fan-in domino OR gates (a) footed standard domino and (b) footless standard domino

evaluation network. This current contention results in increased power dissipation and evaluation delay of standard domino circuits. In fact, there is a trade-off between robustness and performance. As the keeper size increases, the noise immunity improves, but the delay increases, resulting in performance degradation. So, the keeper upsizing is not a suitable way to improve noise immunity.

A leakage tolerant technique that is proposed recently is the Conditional Keeper Logic (CKL) [8], as shown in Fig. 3. This technique employs two keepers (as denoted by K1 and K2). Keeper K1 is a smaller keeper that is initially ON when the evaluation starts (Clock switches to high). The larger keeper (K2) is conditionally turned ON if the precharge node remains high during the evaluation for a longer time than the delay of the delay element. Keeper K1 is ON when the precharge node is high. The conditional keeper technique works as follows: in the precharge phase (clock is low), the dynamic node is precharged to high and the keeper K1 is ON and keeper K2 is OFF. In the evaluation phase (clock is high), initially the keeper K1 is ON and the keeper K2 is OFF. If the evaluation results in discharging of the precharge node, the gate of keeper K2 remains high, and therefore the keeper K2 remains OFF. However, if all the inputs are low in the evaluation phase so that the precharge node is not discharged, then K2 will become ON, strongly keeping the precharge node at the high voltage level. This improves the noise immunity. The noise immunity is further improved by decreasing the delay of the delay element (T_{keeper}); however there are limitations on decreasing T_{keeper}. The reduction of T_{keeper} is done by increasing the sizes of transistors in the delay element; however, this upsizing increases power significantly [3].

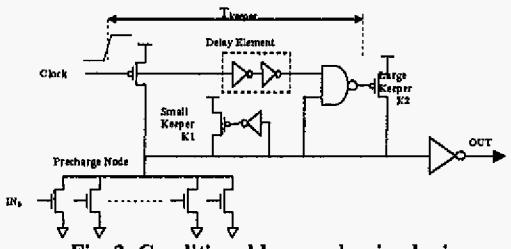

Fig. 3. Conditional keeper domino logic

We propose a new circuit that improves robustness and leakage-tolerance of high fan-in domino gates. Our technique uses smaller keeper transistor that results in less contention between the keeper and evaluation transistors. The performance is improved by utilizing a current mirror circuit in parallel with the evaluation network.

The rest of the paper is organized as follows: in section II, the metric used for noise immunity measurement in our experiments is described. Section III describes our proposed circuit, and the simulation results are shown in section IV. Finally, section V concludes the paper.

II. Noise Immunity Metric

For comparing different circuit techniques for robustness to leakage and noise, we apply identical noises pulses to all inputs of the evaluation network during the evaluation phase, and the amplitude of the resulting noise pulse at the output is measured. The noise immunity metric is the Unity Noise Gain (UNG), defined as the amplitude of the input noise at the input that causes the same amplitude of noise at the output [9]:

$$UNG = \{V_{noise};\ V_{noise} = V_{out}\} \qquad (2)$$

In this technique, a pulse noise emulates cross-talk type of noise at the input. The input noise level can be increased by increasing either the noise pulse duration or amplitude. In our experiments, we change the input noise level by changing its amplitude only.

III. Proposed Leakage Tolerant Domino

Our proposed circuit technique for leakage tolerant domino is illustrated in Fig. 4. The transistor M7 is added to provide stacking effect for leakage reduction in the evaluation phase. However, increased height of transistor stack in the evaluation path increases the evaluation delay. To reduce the evaluation delay, a current mirror (M8) is added in

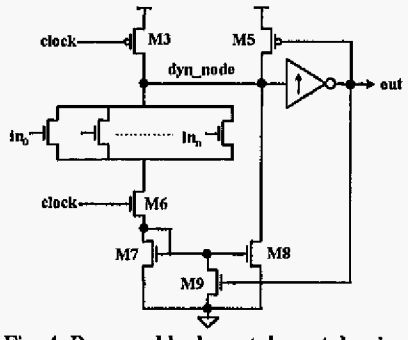

Fig. 4. Proposed leakage tolerant domino

parallel with the evaluation network to increase the discharging current if the evaluation results in discharging of the dynamic node. Transistor M9 provides a feedback from the output to the dynamic node. It is added to be able to fully discharge the dynamic node (to avoid short circuit current on the static inverter) if the dynamic node is discharged in the evaluation phase (output switches to high). The proposed circuit works as follows: when the clock is low, the circuit is in the precharge phase, and the dynamic node (dyn_node) gets precharged to high. The footer transistor (M6) is off and therefore the current mirror (M8) is also off, pulling no current from the dynamic node (dyn_node). In the evaluation phase when the clock is high, this circuit shows excellent noise immunity due to the stacking effect offered by the transistor M7. When the clock is high, if all the inputs are zero, this stacking effect reduces leakage of the evaluation network. However, if at least one of the inputs switches to high, then the mirror transistor pulls large current from the dynamic node resulting in a high to low transition on the dynamic node. In this case, output of the gate transitions to high and the NMOS transistor M9 is turned ON to fully discharge the dynamic node.

Fig. 5 shows typical simulated waveforms of the proposed circuit. The waveforms are obtained by HSPICE simulations of the 64-input OR gate in the worst case I_{off} corner of the 70-nm Berkeley predictive technology models (BPTM) [10] at $110^{\circ}C$ and 0.9 V supply voltage.

IV. Simulation Results

The dynamic OR gates based on the footless standard domino (SD) (Fig.2(b)), conditional keeper logic (CKL) (Fig. 3), and the proposed circuit (Fig. 4) for fan-ins of 8, 16, 32, and 64 were designed in HSPICE at the worst case I_{off} corner of the 70nm Berkeley Predictive Technology node [10]. For the standard domino logic, the keeper ratio (defined in (1)) is increased from 0.18 to 0.8 in order to extract different data points for delay and UNG. For our proposed circuit, the UNG-delay trade off is made by increasing the size of mirror transistor, M8 (Fig. 4).

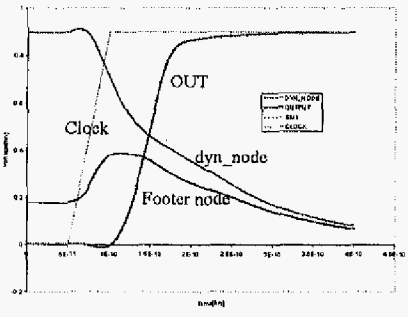

Fig. 5. Simulated waveforms of proposed circuit

The curves of UNG vs. delay for these circuits are illustrated in Fig. 6. As observed from this figure, our proposed circuit exhibits significant increase in UNG compared to the conventional techniques for all fain-ins. It is also evident from Fig. 6 that the effectiveness of the conventional keeper upsizing method is limited in terms of UNG improvement, especially for higher fan-ins, and results in considerable performance degradation. Moreover, for each fan-in, if the UNG is required to be larger than a certain amount, the proposed technique exhibits better performance. For example, it can be observed from Fig. 6 that if the required UNG for a 16, 32, or 64-input domino OR gate is required to be greater than 0.2, then the proposed implementation shows better performance and robustness compared to the standard and conditional keeper domino designs. In the standard and conditional-keeper domino gates, the UNG considerably drops with fan-in increase; however, the UNG does not drop with fan-in increase in the case of the proposed domino. This is due to the fact that the voltage-drop across the footer transistor (M7 in Fig. 4) increases with fan-in increase, causing higher gate switching voltage. Higher gate switching voltage improves noise-immunity. We compare the noise-immunity of the different techniques under same delay (iso-delay UNG). For the proposed design the minimum delay point (the end point of the UNG-delay curves in Fig. 6) is selected and the UNG of that point is compared with the UNG of the corresponding standard and conditional-keeper domino designs at the same delay. Numerical results for UNGs under iso-delay condition are shown in Table 1. The proposed technique shows UNG improvements of 2.0X, 3.7X, 5.4X, and 17.7X compared to the standard domino for fain-ins of 8, 16, 32, and 64, respectively. These improvements are 1.4X, 3.0X, 5.4X, and 10.6X compared to the conditional keeper technique.

These results exhibit the superior noise-immunity of the proposed domino. The noise-immunity improvement is significantly higher for higher fan-in gates. This implies that the proposed technique is more effective for high fan-in gates in terms of performance and UNG improvement. The higher the fan-in is or the higher the required robustness is, the more performance improvement is achieved by the proposed technique. The required UNG depends on technology and surrounding circuits of the domino gates. The proposed circuit can be used for achieving high UNG for wide OR gates with comparable delays to conventional circuits.

V. Conclusions

The tradeoff between performance and robustness for conventional domino gates is achieved by the

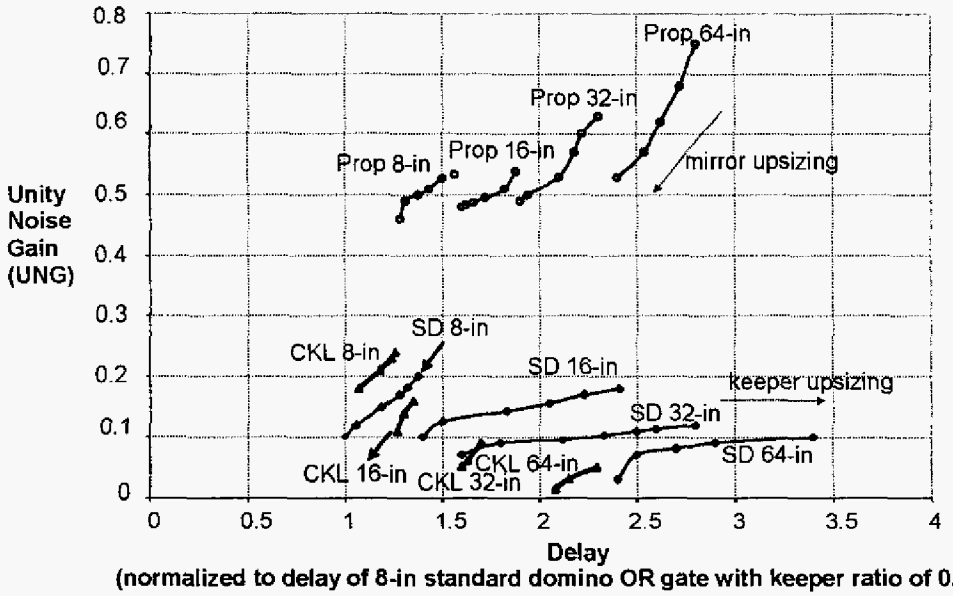

Fig. 6. UNG-delay curves (Prop=proposed technique, CKL= Conditional Keeper Logic, SD= Standard Domino)

Table 1. UNG Comparison under same delay

Fan-in	UNG of standard domino	UNG of conditional-keeper domino	UNG of proposed domino	UNG improvement compared to standard domino	UNG improvement compared to conditional-keeper domino
8	0.17	0.24	0.345	2.0X	1.4X
16	0.13	0.16	0.480	3.7X	3.0X
32	0.09	0.09	0.490	5.4X	5.4X
64	0.03	0.05	0.530	17.7X	10.6X

keeper upsizing. However, because of its significant delay overhead, this method is not a viable solution to maintain noise immunity of domino gates especially for wide OR gates in deep submicron technologies. We have proposed a new circuit technique for improving robustness of high fan-in domino gates while achieving a performance comparable to that of conventional domino gates. The proposed technique shows better improvements for higher fain-ins of gates. The proposed technique enables robust use of high fan-in domino gates in scaled technologies.

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