Dual-Edge Triggered Static Pulsed Flip-Flops

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Abstract

Two Simple structures of low-power Dual-edge triggered Static Pulsed Flip-Flops (DSPFF) are presented in this paper. They are composed of a dual-edge pulse generator and a static flip-flop with equal toggling delays. The static feature of DSPFF avoids unnecessary internal node transitions to reduce power consumption. Simple structure of pulse generator with double-edge triggering is proposed that results in low power dissipation in clock distribution networks. Power consumption of the DSPFF is observed to be the lowest among all high-performance flip-flops and latches. HSPICE simulation results at a frequency of 400MHz show that the proposed DSPFF exhibits more than 24% PDP reduction compared to the hybrid-latch flip-flop (HLFF) and more than 14% PDP reduction compared to conditional-capture flip-flop (CCFF). The proposed DSPFF shows 64% power reduction in comparison to the HLFF and 59% power reduction in comparison to CCFF in practical circuits.

1. Introduction

Since the importance of designing low-power and high performance timing elements has been recognized, many latches and flip-flops have been designed. Hybrid-Latch Flip-Flop (HLFF) is a fast flip-flop and shows negative setup time which provides soft clock edge property, but it consumes large amount of power due to redundant transition of internal nodes. Conditional-Capture Flip-Flop (CCFF) is another high-performance flip-flop which can eliminate redundant internal transitions to minimize power dissipation.

In this paper simple-structure static pulsed flip-flops are proposed which have a small transparency window. The static property of proposed structures avoids unnecessary internal node transitions to reduce power consumption. The proposed pulse generator can be shared among a group of flip-flops to reduce the power and area overhead of pulse generation. Proposed flip-flops present low power dissipation in clock distribution network. Double-edge triggering is a technique incorporated into the flip-flops and latches for significant clock power reduction [1,2]. Double-edge triggering feature applied in proposed flip-flops helps to reduce the clock frequency by 50%, and therefore extra energy saving can be obtained in the clock distribution network.

The remainder of this paper is organized as follows. In sections 2, the high-performance flip-flops and lathes are reviewed. Sections 3, explains the proposed dual-edge triggering static pulsed flip-flops. In section 4, extensive simulation results of individual flip-flops and latches and their comparisons are presented. Finally, the conclusion of the paper appears in Section 5.

2. High performance flip-flops and latches

Figure 1 shows the schematic diagram of representative high performance flip-flops and latches. They are Hybrid Latch-Flip-Flop (HLFF) [3], modified Sense Amplifier-based Flip-Flop (SAFF) [4], and differential Conditional-Capture Flip-Flop (CCFF) [5]. HLFF as shown in Figure 1(a) is actually a latch with a brief transparency period. The major advantage of HLFF is the small data to output latency and the soft-clock edge property. HLFF is a single-ended output flip-flop and it shows relatively large clock power consumption, moreover it consumes large amount of power due to redundant transition of internal nodes at low data switching activities. SAFF as shown in Figure 1(b) incorporates a pre-charged sense amplifier and a symmetric latch topology that significantly reduces delay and improves driving capability. It has redundant transition of internal nodes at low data switching activities due to pre-charged sense amplifier structure. Conditional-Capture Flip-Flop (CCFF) which is shown in Figure 1(c) achieves statistical power reduction by eliminating internal redundant transitions. CCFF needs too many transistors for conditional capturing and it shows large clock load.

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3. Static Pulsed Flip-flops

Edge-triggered latches create a narrow sampling window to overcome race problem in comparison to simple latch structures. Therefore this idea was applied to our simple static flip-flop structures. Double-edge triggered flip-flops can latch the data on both rising and falling edge of the clock. Thus, the clock frequency is reduced by half while the data throughput is preserved. Figure 2 shows two proposed static pulsed flip-flops structures. They have the same pulse generator circuit as shown in figure 2(c). The pulse generator consists of four inverters which generate delayed and inverted clock signals, *CLK2* and *CLK3*, along with two NMOS transistors for pulse generation. Delayed clock signal *CLK2* which is the inverse of *CLK* is applied to the drain of *MN8* while the clock (*CLK*) controls the gate of *MN8*. When rising edge of the clock signal begins, *CLK2* is high and the pass transistor *MN8* charge the *PULS* node therefore a narrow sample window is generated at the rising edge of the clock signal. Delayed clock signal *CLK3, CLK1* and pass transistor *MN9* create another pulse at the falling edge of the clock signal in the same manner. Therefore the pulse signal is generated at both rising and falling edge of the clock as shown in Figure 3. In Figure 2(a) the *PULS* signal applied to the NMOS transistor *MN1* creates a narrow transparency window in which data inputs can affect the state of static nodes *SB* and *S* via NMOS transistors *MN2* and *MN3*. The PMOS transistor *MP5 (MP4)* pulls *S (SB)* node up to *Vdd*. By proper sizing of the NMOS and PMOS transistors of the output inverters and transistors *MN2, MN3, MN4 and MP5*, the proposed flip-flop structure shows equal low to high and high to low output latency, similar to SAFF and CCFF structures.

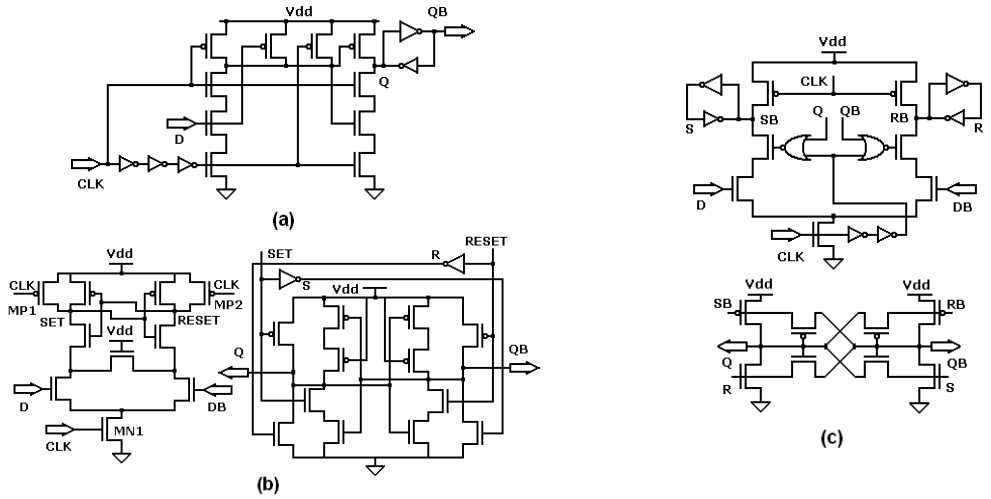

Figure 1. High-performance flip-flops and latches: (a) HLFF (b) SAFF (b) CCFF

In Figure 2(b) another simple structure is proposed for dual-edge triggered static pulsed flip-flop. Pass transistors *MN2* and *MN3* contribute in data capturing during the pulse window with *PULS* signal. Since data inputs have direct access to static nodes *SB* and *S* through *MN2* and *MN3*, this structure shows smaller delay than the former one. For distinction of these two dual-edge triggered static pulsed flip-flops the first flip-flop was named as DESPFF and the second one as DSPFF. The node that stays at zero voltage (*SB* or *S*) can be floated when the pulse is finished and it could result in short-circuits current on the following inverter or even functional failure. Using two weak NMOS transistors *MN6* and *MN7* the nodes *SB* and *S* will not be floated at anytime. In these structures the generated pulse has a little latency relative to the clock edge. This provides negative setup time for the proposed flip-flops. The pulse generator can be shared among a group of flip-flops to reduce the power and area overhead of pulse generation. Figure 4 shows simulated waveforms of proposed DSPFF. In Figure 4(a) transition of Q at rising edge of the clock and in Figure 4(b) transition of Q at falling edge of the clock is shown. It is obvious that both outputs Q and QB have the same data to output latency. Therefore the proposed dual-edge triggered static pulsed flip-flops present symmetric output toggling like other high performance flip-flops.

4. Simulation results and comparisons

All the flip-flops and latches were designed using the BPTM0.18µm Process technology models [6] with a supply voltage of 1.8V. The designs were optimized for a clock frequency of 400MHz and data switching activity equal to 0.5. A load capacitance of 100fF was used for all

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outputs. Transistor sizing was optimized using an iterative procedure with the objective of achieving high speed and low power (minimum Power-Delay Product (PDP)) for all high-performance flip-flops and latches.

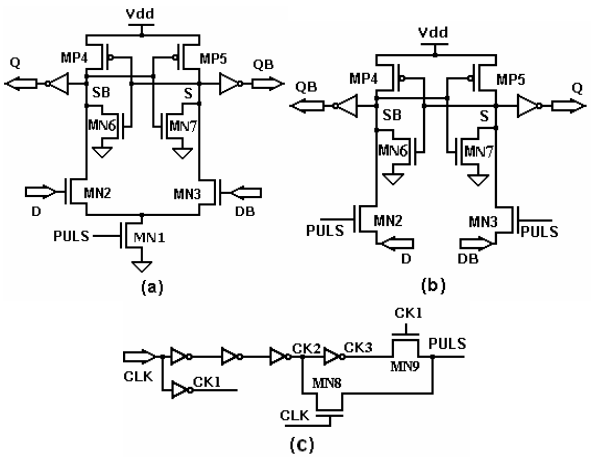

Figure 2. Proposed dual-edge triggered static pulsed flip-flop structures: (a) DESPFF (b) DSPFF.

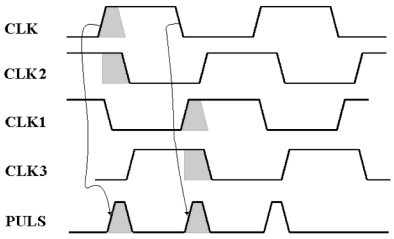

Figure 3. Pulsed clock generation for proposed flip-flops.

Table 1 summarizes the numerical results for all high-performance flip-flops along with the proposed designs. The proposed static pulsed flip-flops show larger data to output latency but smaller power consumption in comparison to other high-performance flip-flops and latches. Both proposed designs show symmetric output transitions like CCFF and SAFF. Moreover the negative setup time of the proposed designs provides soft-clock edge property for overcoming clock skew-related cycle time loss. The PDP reduction of DESPFF and DSPFF are 14.6% and 11.9% respectively in comparison to CCFF which shows the lowest PDP among all other flip-flops. Comparison to HLFF, these values are 24.8% and 22.3%, respectively.

Power contribution of three main sources of power dissipation including internal power dissipation, local clock power dissipation, and local data power dissipation were measured for data switching activity of 0.5. As shown in Figure 5, the DESPFF and DSPFF present the lowest local clock power dissipation while CCFF consumes large amount of clock power due to its high clock loads. Total power consumptions of DESPFF and DSPFF are 27.6% and 23.5% lower than CCFF. These values are 35.9% and 32.2% for comparison with HLFF.

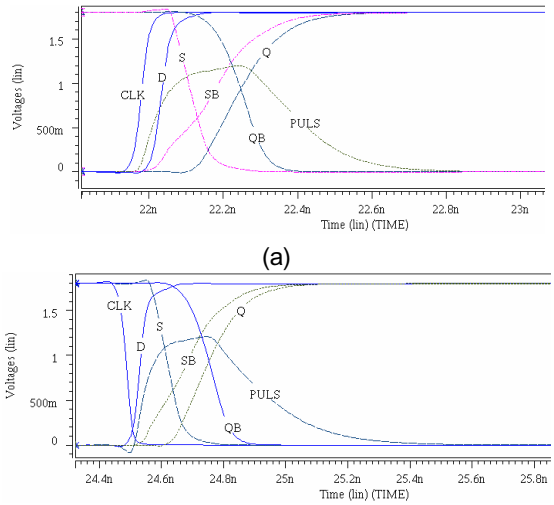

Figure 4. Simulated waveforms of proposed flip-flops: (a) rising edge of clock (b) falling edge of clock

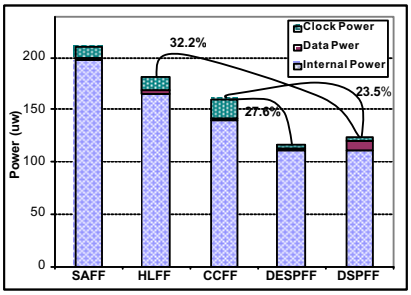

Figure 5. Detailed power consumption of different flip-flops and latches.

Proposed pulse generation circuits present much power saving in clock distribution network. Assuming the clock network power is dominated by the power due to clock input capacitances of flip-flops, the clock network power consumption is extrapolated and shown in Figure 6. Due to less clock input capacitance and operating at half the clock frequency in the proposed dual-edge triggered flip-flops, they show significant reductions in clock network power dissipation. As shown in Figure 6, both DESPFF and DSPFF present 83.9% and 77.0% power savings in clock network in comparison to CCFF and HLFF, respectively. Figure 7 shows power as a function of data switching activity for different flip-flops and latches. The proposed single edge-triggered static pulsed flip-flops have the lowest power consumption at all switching activities among all flip-flops. DESPFF and DSPFF have static nature and this feature avoids unnecessary internal node transitions at low data switching activities, and

therefore they show small power consumption at low data switching activities.

A lower power scheme of proposed designs at different data switching activities can be obtained by implementing an 8-bit counter. An 8-bit counter presents different switching activities from low values up to unity switching activity. Figure 8 shows power consumption of the counters designed with different flip-flops. As shown in Figure 8 the proposed structures of the static pulsed flip-flops again show lowest power consumption while SAFF shows highest amounts of power consumption because of its high power dissipation at all data switching activities. DESPFF shows 59.6% and 42.1% power reduction in comparison to HLFF and CCFF, respectively. The power reduction values will be 64.0% and 48.3% for DSPFF in comparison to HLFF and CCFF, respectively. These values can be increased by sharing the pulse generator among a group of flip-flops to reduce the power. The area of DSPFF is the lowest among all high-performance flip-flops.

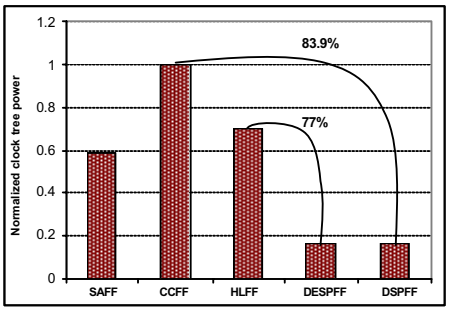

Figure 6. Normalized clock network power consumption comparisons

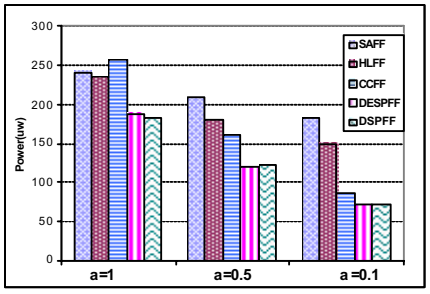

Figure 7. Power vs. data switching activity at 400MHz.

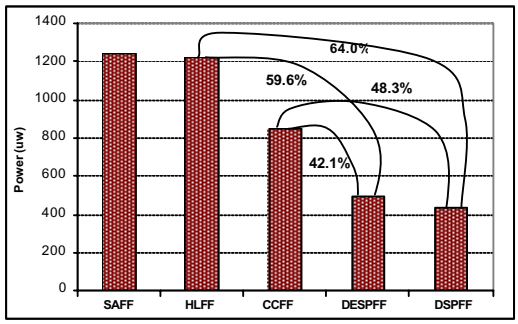

Figure 8. Comparison of power consumption of counters

5. Conclusions

Two simple dual-edge triggered static pulsed flip-flops were proposed for low-power and high-performance applications. Based on our simulation results, the proposed structures have equal high to low and low to high delay. The pulse generation circuits used in the proposed flip-flops show significant amount of power saving on clock tree. The low power consumption of the proposed static pulsed flip-flops at all switching activities suggests extensive using of these structures for future low-power applications.

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Table 1: Numerical results at 50% data switching activity with 400MHz clock frequency

	D-Q(QB) (pS)	Setup time (pS)	Hold time (pS)	Power (μW)	PDP (fJ)	Norm. PDP	Device count	Total Width (μm)
CCFF	156.8	-26.5	88.0	160.3	25.13	0.756	35	56.3
SAFF	157.7	-18.8	56.0	210.6	33.21	1.000	26	46.2
HLFF	157.5	-55.5	113.0	181.0	28.50	0.858	20	47.0
DESPFF	184.7	-165.3	327.0	116.0	21.42	0.645	24	40.3
DSPFF	180.5	-174.8	298.0	122.6	22.13	0.666	25	35.3

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