High Performance and Low Power Domino Logic Using Independent Gate Control in Double-Gate SOI MOSFETs

Hamid Mahmoodi, Saibal Mukhopadhyay, and Kaushik Roy
Dept. of ECE, Purdue University, West Lafayette, IN-47907
Email: < mahmoodi, sm, kaushik>@ecn.purdue.edu, Tel: (765) 494-0750

1. Introduction

Double-gate SOI MOSFETs (DGMOS) have been shown to be very scalable due to less short channel effects and intrinsic body (no random dopant fluctuations effect) [1]. In DGMOS transistors, usually back and front gates are connected together (*connected front and back gates*) to achieve more ON current (I_{on}) and reduce short-channel effects. Larger I_{on} is helpful in reducing circuit delay in critical paths. However, for transistors in non-critical paths, small transistor sizing (less I_{on}) is used to reduce power dissipation. In addition to minimal sizing, single gate driving (*independent gate control*) of DGMOS can reduce gate capacitance and therefore power dissipation on non-critical transistors. In this paper, the concept of independent gate control is applied to domino logic for improving circuit performance and reducing power consumption. Domino circuits are widely used for high-speed implementation of performance critical circuits [2].

2. DGMOS Device Characteristics

Fig. 1 shows the DGMOS device used in this paper. This is a fully depleted symmetric device with L_{gate}=50nm, L_{eff}=35nm, T_{oxf}=T_{oxb}=2.5nm, and T_{si}=10nm. The device and circuit simulations were carried out using the device simulator MEDICI. Fig. 2, shows the IV characteristics of the designed device for the cases of *connected front and back gates* (VFgate=VBgate) and *independent gate control* (with back gate bias voltage of zero). The I_{on} reduces in the case of independent gate control; however the off current (I_{off}) remains same.

3. Independent Gate Control in Domino Logic

Fig. 3 shows a domino OR gate implemented using DGMOS devices with connected front and back gates for all devices. In this paper, we refer to this scheme as conventional implementation. The first scheme (Fig. 3-a) is a footless domino gate, and the second scheme (Fig. 3-b) uses a footer transistor [2]. In a cascaded chain of domino gates, footless topology is preferred for very high performance designs [2]. The static inverter is skewed for fast low-to-high transition to improve performance [2].

In scenarios where there are parallel transistors in non-critical paths with common drain and source nodes, it is possible to combine the two transistors into a single DGMOS transistor with back and front gates separately controlled by different inputs. This is the case in domino gates for the precharge and keeper transistors (Fig. 3). These two transistors are not in critical delay path, which is the evaluation path (NMOS evaluation network followed by the PMOS of the inverter). Therefore, these two transistors can be merged into a single DGMOS device as shown in Fig. 4. This merging has several advantages: (a) the clock load capacitance (gate of precharge transistor) decreases, (b) the output load capacitance (gate of keeper transistor) decreases, and (c) parasitic capacitances on the precharge node (X) decrease. All of these result in less power consumption and higher performance (shorter delay of the evaluation path).

The performance of domino logic can be further improved by skewing the inverter driving the output for fast low-to-high transition. In order to skew the inverter in this direction, the back gate of the NMOS transistor can be connected to ground (zero voltage) as shown in Fig. 5. Moreover, the gate capacitance loading the precharge node (X) reduces, further helping for less power dissipation. Having a back gate bias of zero voltage for the NMOS however is not desirable in the precharge phase as it results in a slow precharging. In another words, the inverter is desired to be skewed for low-to-high transition during the evaluation phase and for high-to-low transition during the prechrage phase. These can be simultaneously achieved by connecting the back-gate of the NMOS transistor to the inverted clock signal (CKB), as shown in Fig. 6. In this way, the inverter is dynamically skewed for the preferred transition. However, this technique has some power overhead due to the extra clock load.

4. Simulation Results and Comparisons

All the proposed circuit ideas are simulated in MEDICI using the designed device (Fig. 1). Fig. 7 shows typical simulation waveforms of the designed domino circuits. Fig. 8 shows comparison of evaluation delay of the conventional DGMOS domino (Fig. 3) and the proposed DGMOS domino circuits (Fig. 4-6). The keeper width in the case of the proposed schemes represents the width of the Merged Prechare/Keeper (MPK) transistor. The width of the precharge transitor in the conventional domino circuits is kept at minimum width (100nm). The improvement in delay is quite significant for both the footless and footed schemes. Moreover, the delay in the proposed schemes is less sensitive to the keeper size. The MPK & DSI scheme (Fig. 6) shows the least delay. Depending on the keeper size, delay reduction of 30% to 60% for footless domino and 40% to 80% for footed domino is observed. Fig. 9 shows power comparison of different DGMOS

*This work is supported in part by Semiconductor Research Corporation under contract no. 1078.

0-7803-8497-0/04/$20.00 ©2004 IEEE

domino logic schemes. Due to reduced gate and parasitic capacitances, the proposed schemes show significant power reduction as well. The MPK & SSI scheme (Fig. 5) shows the least power dissipation. The power dissipation of the dynamically skewed scheme (Fig. 6) is a little higher than the MPK and MPK & SSI schemes, due to extra clock signal power overhead. Power savings of 25% to 42% for footless domino and 0% to 60% for footed domino is observed. Fig. 10 shows the precharge delay comparisons. The proposed schemes show an increase in precharge delay due to reduced strength of the precharge transistor; however this delay is not a critical delay in domino logic. Moreover, the MPK & DSI scheme (Fig. 6) alleviates this problem by dynamically changing the skew of the inverter for the preferred transition.

5. Conclusion

Independent gate control of DGMOS devices can be effectively used in circuit design for reducing power dissipation and improving performance in DG-SOI.

References

[1] L. Chang, et. al., "Extremely Scaled Silicon Nano-CMOS Devices," Proceedings of the IEEE, Vol. 91, Issue: 11, pp. 1860–1873, Nov. 2003

[2] Design of High-Performance Microprocessor Circuits, A. Chandrakasan, W.J. Bowhill, and F. Fox, Piscataway, NJ, USA: IEEE Press, 2001.

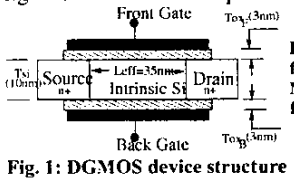
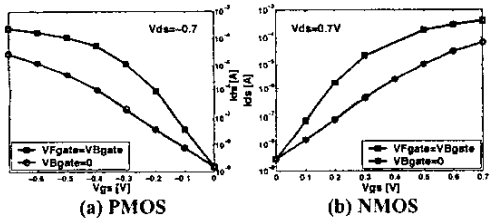
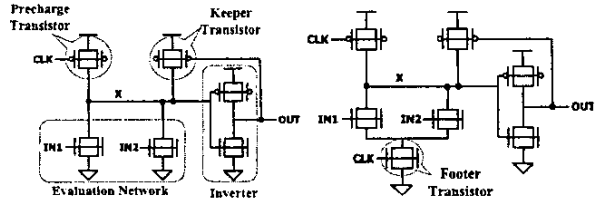


Fig. 1: DGMOS device structure



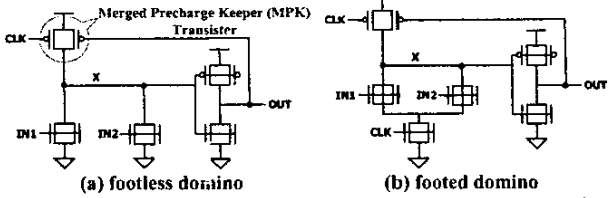
(a) PMOS (b) NMOS

Fig. 2: Ids-Vgs characteristics



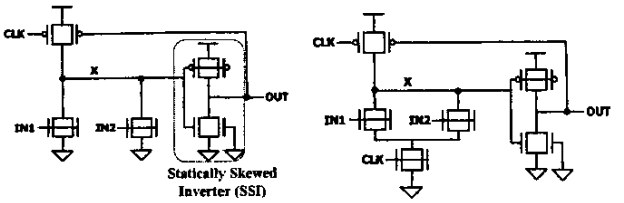
(a) footless domino (b) footed domino

Fig. 3: Conventional Domino OR gate in DGMOS: back and front gates connected together for all devices



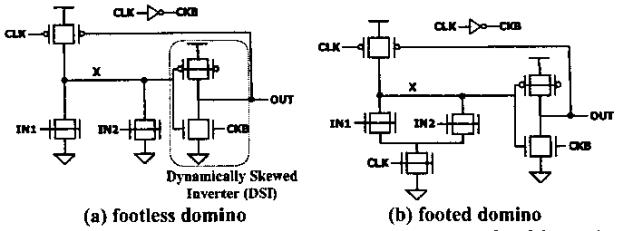
(a) footless domino (b) footed domino

Fig. 4: Merged Precharge/Keeper (MPK) scheme in DGMOS Domino



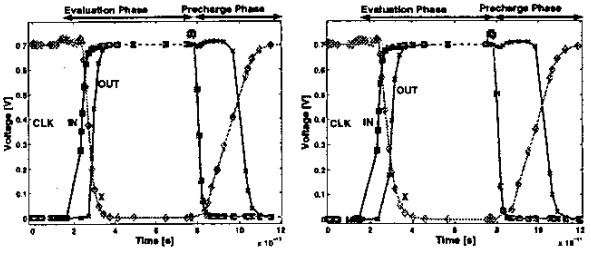
(a) footless domino (b) footed domino

Fig. 5: MPK & Statically Skewed Inverter (SSI) in DGMOS Domino



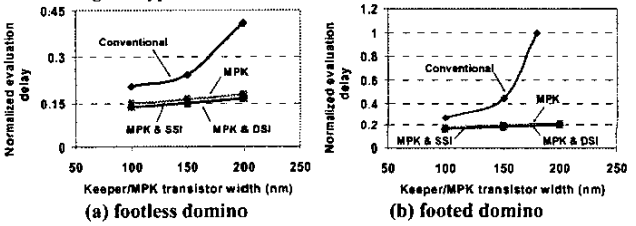
(a) footless domino (b) footed domino

Fig. 6: MPK & Dynamically Skewed Inverter (DSI) in DGMOS Domino



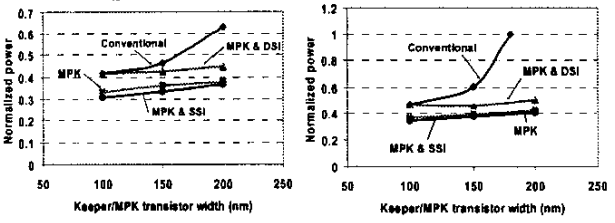
(a) footless domino (b) footed domino

Fig. 7: Typical simulation waveforms of DGMOS Domino



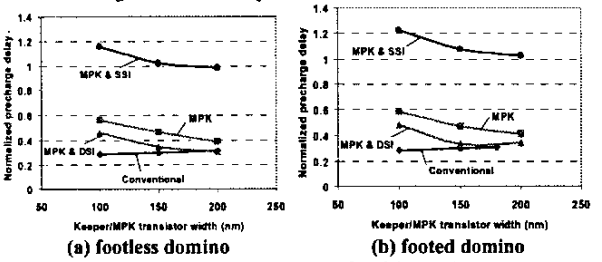
(a) footless domino (b) footed domino

Fig. 8: Evaluation delay of DGMOS Domino



(a) footless domino (b) footed domino

Fig. 9: Power dissipation of DGMOS Domino



(a) footless domino (b) footed domino

Fig. 10: Precharge delay DGMOS Domino