Modeling and Estimation of Failure Probability due to Parameter Variations in Nano-scale SRAMs for Yield Enhancement *

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ABSTRACT

In this paper we have analyzed and modeled the failure probabilities (access time failure, read/write stability failure, and hold stability failure in the stand-by mode) of SRAM cells due to process parameter variations. A method to predict the yield of a memory chip designed with a cell is proposed based on the cell failure probability. The developed method can be used in the early stage of a design cycle to optimize the design for yield enhancement.

1. INTRODUCTION

Increasing inter-die statistical variations in the process parameters (channel length (*L*), width (*W*), and transistor threshold voltage (*Vt*)) has emerged as a serious problem in the nano-scaled circuit design [1]. The inter-die parameter variations, coupled with the intrinsic on-die variation in Vt due to random dopant fluctuation, can result in failure of SRAM cells [1]. A cell failure can occur due to: (a) an increase in the cell access time (access time failure), (b) unstable read/write operations (read/write stability failure), or (c) failure in the data holding capability of the cell at a lower supply voltage (hold stability failure in the stand-by mode). A failure in any of the cells in a column (or row) of the memory will make that column (or row) faulty. If the number of faulty columns (or rows) in a memory chip is larger than the number of redundant columns (or rows), then the chip is considered to be faulty. Hence, the failure probability of a cell is directly related to the yield of a memory chip. Consequently, estimation of the failure probability for a cell is necessary in the design phase to ensure a good yield. In this paper, we have developed a method to predict the yield of a memory chip under inter-die variation of *L*, *W* and *Vt* by estimating the failure probability of the cell considering intra-die parameter variation. The method is developed considering intra-die Vt variation (principally due to random dopant fluctuation) and can be extended to include on-die random variation in L and W. In particular, we have

- Modeled the access time, the read stability, the write stability, and the hold stability failures of a cell due to process variation.
- Developed a method to estimate the failure probability of a memory and to predict the yield of a memory chip.
- Presented a statistical analysis of the impact of circuit (transistors sizing) and architecture (# of rows and columns) on the cell failure probability and memory yield.

2. DEVICE CHARACTERITICS

In our SRAM cell (Fig.1) we have used transistors of 50nm gate length (*Leff=25nm*) designed using MEDICI [2], [5]. In our analysis, we have used the short channel MOSFET theory to model the currents and threshold voltage considering the device geometry and doping profile [3], [4]. Fig. 2 shows the Id-Vg characteristics of the designed transistors.

3. ESTIMATION of CELL FAILURE PROBABILITY (P_F) and YIELD PREDICTION

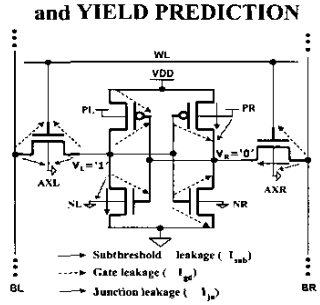


Fig. 1: SRAM Cell

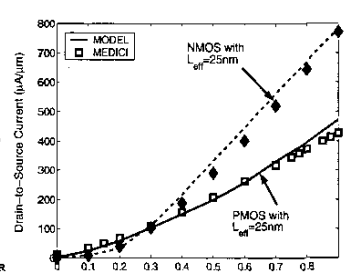


Fig. 2: Device Characteristics

*This work is supported in part by Semiconductor Research Corp., DARPA PACC program.

A failure in an SRAM cell can occur due to: (a) an increase in the access time of the cell resulting in a violation of delay requirement, defined as *access time failure*, (b) destructive read (*read failure*) and/or unsuccessful write (*write failure*), resulting in a dynamic stability failure (Fig. 3) and, (c) the destruction of the cell content in the standby mode with the application of a pre-specified (designed) lower supply voltage (V_{HOLD}), known as *hold-stability failure* (Fig. 3). In a die, failures are principally caused by the mismatch in the device parameters (*L, W, Vt*) of different transistors (intra-die) in the cell. Such device mismatch modifies the strength of the different transistors resulting in different failure events. The principal source of the device mismatch is the intrinsic fluctuation of the Vt of different transistors due to random dopant effect [1]. Hence, in this work we have considered the Vt variation as the major source of intra-die variation while estimating the failure probabilities. The proposed method can also be extended to include L and W variation (or the impact of *L* and *W* variations can also be represented as an additional contribution to the Vt variation).

3.1. Distribution of the Intrinsic Vt Variation (δVt)

To estimate the failure probability, the threshold voltage (Vt) of the cell transistors are considered as six *independent random variables* (RV) [1]. The probability distribution function (pdf) of Vt fluctuation (δVt) of each transistor is assumed to be Gaussian (mean=0). The standard deviation (σ_{Vt}) depends on the manufacturing process, doping profile, and the transistor size. In the proposed method, σ_{Vt} for a minimum sized transistor (σ_{Vt0}) is an input parameter and the dependence of σ_{Vt} on the transistor size is given by [4]:

$$\sigma_{Vt} = \sigma_{Vt0}\sqrt{(L_{min}/L)(W_{min}/W)} \qquad (1)$$

3.2. Access Time Failure (A_F)

The cell access time (T_{ACCESS}) is defined as the time required to produce a pre-specified (Δ_{MIN}~$0.1V_{DD}$) voltage difference between two bit-lines (bit-differential). If due to Vt variation, the access time of the cell is higher than the maximum tolerable limit (T_{MAX}), an access time failure is said to have occurred. The probability of access time failure (P_{AF}) of a cell is given by:

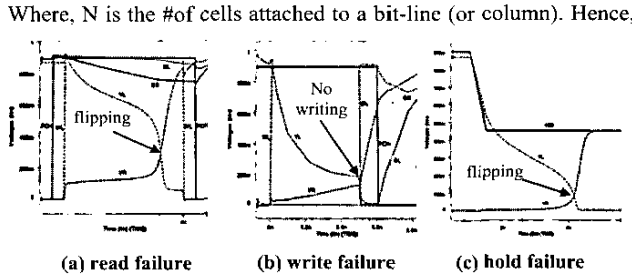
$$P_{AF} = P(T_{ACCESS} > T_{MAX}) \qquad (2)$$

While reading the cell storing V_L='*1*' and V_R='*0*' (Fig.1, Fig.3), bit-line BR will discharge through AX_R and N_R (by the current I_{BR}). Simultaneously, BL will discharge by the gate leakage, the subthreshold leakage, and the junction leakage of AX_L of all the cells (I_{BL}) connected to BL. The discharging currents I_{BR} and I_{BL} are given by:

$$I_{BR} = I_{dsatAXR} + \sum_{i=1,..,N}\left[I_{gdAXR(i)} + I_{jnAXR(i)}\right] \qquad (3a)$$

$$I_{BL} = \sum_{i=1,..,N}\left[I_{gdAXL(i)} + I_{jnAXL(i)} + I_{subAXL(i)}\right] \qquad (3b)$$

Where, N is the #of cells attached to a bit-line (or column). Hence,



(a) read failure **(b) write failure** **(c) hold failure**

Fig. 3: Unstable read and write operations

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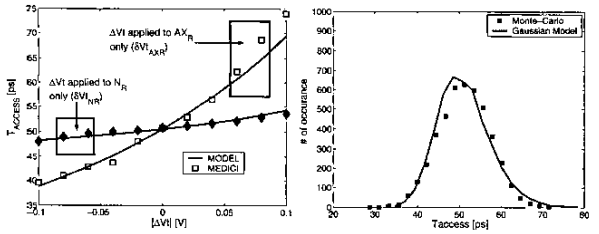


(a) T_{ACCESS} variation with δVt (b) distribution of T_{ACCESS}

Fig. 4: Variation and distribution of T_{ACCESS} with variation in δVt

T_{ACCESS} can be accurately obtained by solving:

$$T_{ACCESS} = \int_{V_{DD}}^{V_{DD}-\Delta V_{BL}-\Delta_{MIN}} \frac{C_{BR}dV_{BR}}{I_{BR}} = \int_{V_{DD}}^{V_{DD}-\Delta V_{BL}} \frac{C_{BL}dV_{BL}}{I_{BL}} \quad (4)$$

where, $C_{BR/BL}$ is the bit-line capacitance that includes the diffusion capacitance (measured using MEDICI [5]) (C_{jn}) of the access transistors and the interconnect capacitances (C_{IC}). To simplify the above calculation, for the estimation of P_{AF}, we assume that $I_{dsatAXR}$ is constant (valid for small ΔV_{BR} since AX_R is in saturation) and I_{gd}, I_{jn} and I_{sub} are constant at their values for $V_{BL}=V_{DD}$ (valid for small ΔV_{BR} and ΔV_{BL}). Hence, ΔV_{BR} and ΔV_{BL} are linear functions of time (Fig. 3a). We further assume that $C_{BL}=C_{BR}=C_B$, $I_{gdAXR(i)}= I_{gdAXL(i)}$ and $I_{jnAXR(i)}= I_{jnAXL(i)}$ (since they are not a strong function of Vt). Using these assumptions, T_{AC} can be given by:

$$T_{ACCESS} = \frac{C_{BR}C_{BL}\Delta_{MIN}}{C_{BL}I_{BR} - C_{BR}I_{BL}} = \frac{C_B\Delta_{MIN}}{I_{dsatAXR} - \sum_{i=1,..,N} I_{subAXL\,(i)}} \quad (5)$$

The access time given by (5) closely follows the MEDICI simulation result (Fig. 4a). T_{ACCESS} principally depends on Vt of AX_R and N_R which determines $I_{dsatAXR}$. ($\sum I_{subAXL(i)}$ is approximated as $N \times E[I_{subAXL}]$, where, $E[I_{subAXL}]$ is the expected value of I_{subAXL} considering random variation in δVt_{AXL}). From Fig. 4b, it can be observed that, the distribution of T_{ACCESS} (considering variation in independent RVs δVt_{AXR} and δVt_{NR}) is approximately Gaussian in nature. Hence, we estimate the pdf of T_{ACCESS} as a Gaussian RV with mean (η_{TAC}) and standard deviation (σ_{TAC}) given by [6]:

$$\eta_{TAC} = \left[T_{ACCESS} + \frac{1}{2}\left(\frac{\partial^2 T_{ACCESS}}{\partial(\delta Vt_{AXR})^2}\sigma^2_{AXR} + \frac{\partial^2 T_{ACCESS}}{\partial(\delta Vt_{NR})^2}\sigma^2_{NR} \right) \right]_{\eta_{AXR},\eta_{NR}}$$

$$\sigma^2_{TAC} = \left[\left(\frac{\partial T_{ACCESS}}{\partial(\delta Vt_{AXR})} \right)^2 \sigma^2_{AXR} + \left(\frac{\partial T_{ACCESS}}{\partial(\delta Vt_{NR})} \right)^2 \sigma^2_{NR} \right]_{\eta_{AXR},\eta_{NR}} \quad (6)$$

where, $\sigma_{AXR/NR}$ is the standard-deviation and $\eta_{AXR/NR}$ (=0) is the mean of the δVt distribution of the transistors AX_R/N_R. The derivatives can be estimated numerically. The distribution using (6) closely matches the exact distribution (Fig. 4b). Using the derived pdf ($f_{TACCESS}(t_{ACCESS})$), P_{AF} can be estimated as:

$$P_{AF} = \int_{t_{ACCESS}=T_{MAX}}^{\infty} f_{TACCESS}(t_{ACCESS})d(t_{ACCESS}) = 1 - F_{TACCESS}(T_{MAX}) \quad (7)$$

where, $F_{TACCESS}(t_{ACCESS})$ is the cumulative distribution function (cdf) of a Gaussian pdf. P_{AF} of a cell using the model closely matches the one obtained using Monte-carlo simulation (Table-1).

3.3. Read Stability Failure (R_F)

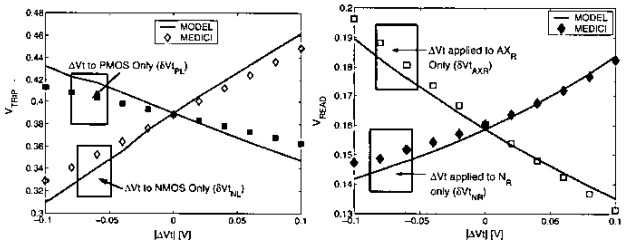


Fig. 5: Variation of (a) V_{TRIP} of P_L-N_L and (b) V_{READ}, with δVt applied to different transistors

While reading the cell shown in Fig. 1 (V_L='1' & V_R='0'), V_R increases due to the voltage divider action of AX_R and N_R to a positive value V_{READ}. If V_{READ} is higher than the trip point of the inverter P_L-N_L (V_{TRIPRD}) then the cell flips after reading the cell (Fig.3(a)) [7]. This represents a *read failure* (R_F) event. Hence, the read-failure probability (P_{RF}) is given by:

$$P_{RF} = P\left[V_{READ} > V_{TRIPRD}\right] \quad (8)$$

V_{READ} can be obtained by solving KCL simultaneously at node R and L as given by:

$$\text{At } R \equiv I_{dsatAXR} + I_{gsAXR} + I_{subPR} + I_{gdPR} + I_{jnPR} + I_{gdNR} + I_{gdNL} + I_{gdPL} + I_{gsPL} = I_{dlinNR} + I_{jnNR} + I_{jnAXR} \quad (9)$$

$$\text{At } L \equiv I_{dsNL} + I_{jnNL} + I_{gdNL} + I_{gdPL} = I_{dsPL} + I_{jnPL} + I_{dlinAXL}$$

Neglecting the leakage current components to node R, we have [7]:

$$\text{At } R \equiv I_{dsatAXR} = I_{dlinNR} \quad (10)$$

Similarly, V_{TRIPRD} can be obtained by solving [7]:

$$I_{dsatNL}(V_{TRIPRD}, V_{TRIPRD}, gnd) \approx I_{dsatPL}(V_{TRIPRD}, V_{TRIPRD}, V_{DD}) \quad (11)$$

Fig. 5 shows that V_{TRIPRD} (obtained using (11) and MEDICI simulation) is a linear function of independent RV's δVt_{NL} & δVt_{PL}. Similarly, V_{READ} (obtained using (10) and MEDICI simulation) is a linear function of independent RV's δVt_{AXR} & δVt_{NR}. Hence, the pdf of V_{READ} (=$f_{RD}(v_{READ})$) and V_{TRIP} (=$f_{TRIP}(v_{TRIP})$) can be approximated as Gaussian distributions (since δVts are Gaussian) with the means the variances obtained using (6) (Fig. 6a, 6b). P_{RF} is given by:

$$P_{RF} = P\left[Z \equiv \left(V_{READ} - V_{TRIPRD}\right) > 0\right] = 1 - F_Z(0)$$

$$\text{where, } \eta_Z = \eta_{V_{READ}} - \eta_{V_{TRIP}} \text{ and } \sigma_Z^2 = \sigma^2_{V_{READ}} + \sigma^2_{V_{TRIPRD}} \quad (12)$$

The estimated value of P_{RF} closely follows the values obtained from Monte-Carlo simulations (Table-1).

3.4. Write Stability Failure (W_F)

While writing a '0' to a cell storing '1', the node V_L gets discharged through BL to a low value (V_{WR}) determined by the voltage division between the PMOS P_L and the access transistor AX_L [7]. If V_L can-not be reduced below the trip point of the inverter P_R-N_R (V_{TRIPWR}), within the time when word-line is high (T_{WL}), then a write failure occurs (Fig. 3b). The write-failure probability (P_{WF}) is given by:

$$P_{WF} = P\left[\left(T_{WRITE} > T_{WL}\right)\right] \quad (13)$$

where, T_{WRITE} is the time required to pulldown V_L from V_{DD} to V_{TRIPWR}. T_{WRITE} is obtained by solving:

$$T_{WRITE} = \begin{cases} \left| \int_{V_{DD}}^{V_{TRIP}} \frac{C_L(V_L)dV_L}{I_{in(L)}(V_L) - I_{out(L)}(V_L)} \right|; & if\,(V_{WR} < V_{TRIPWR}) \\ \infty; & if\,(V_{WR} \geq V_{TRIPWR}) \end{cases} \quad (14)$$

$I_{in(L)}$ = current into L $\approx I_{dsPL}$, $I_{out(L)}$ = current out of L $\approx I_{dsAXL}$

where C_L is the net capacitance at the node L. V_{WR} can be obtained by simultaneously solving KCL at node L & R. However, neglecting the leakage contributions, we can obtain V_{WR} by solving $I_{dlinAXL} \approx I_{dsatPL}$ (assuming V_{WR} is low enough so that AX_L is in linear region and P_L is in saturation region). V_{TRIPWR} can be obtained by solving for trip-point of the inverter P_R-N_R using (11). T_{WRITE} obtained using (14) closely matches the MEDICI simulation result with Vt variation of different transistors (Fig. 7a). T_{WRITE} is a strong function of the RVs δVt_{PL}, δVt_{NR}, δVt_{PR} & δVt_{AXR}. Using (6) we can estimate the mean (η_{TWR}) and the standard-deviation (σ_{TWR}) and approximate the pdf as a Gaussian one ($f_{WR}(t_{WR})$) (Fig. 7b). However, most of the write-failures originate from the 'tail' of the

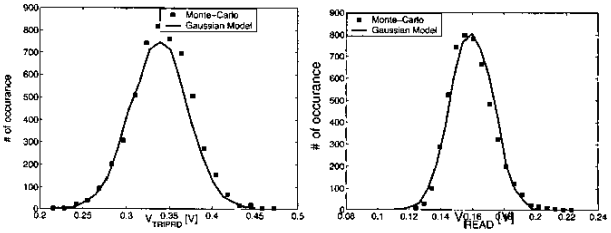
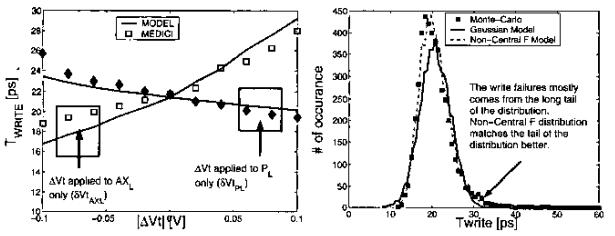


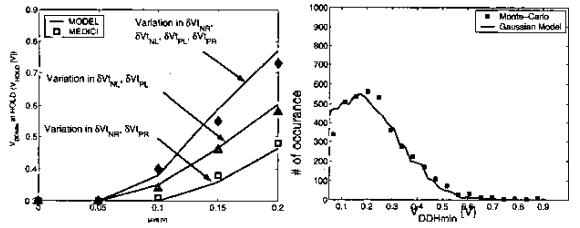
Fig. 6: Distributions of (a) V_{TRIP} of P_L-N_L and (b) V_{READ}



(a) T_{WRITE} variation with δVt (b) distribution of T_{WRITE}

Fig. 7: Variation and distribution of T_{WRITE} with variation in δVt

distribution function. Hence, to improve the accuracy of the model



(a) V_{DDHmin} variation with δVt (b) distribution of V_{DDHmin}

Fig. 8: Variation of and Distribution of V_{HOLD}. In (a) δVt applied in the directions: (δVt_{NR}>0, δVt_{PR}<0, δVt_{NL}<0, δVt_{PL}>0)

at the tail region, we can use a non-central F distribution [6]. Using the pdf (Gaussian/non-central F) of T_{WRITE}, the P_{WF} is given by:

$$P_{WF} = \int_{t_{WR}=T_{WL}}^{\infty} f_{WR}(t_{WR})d(t_{WR}) = 1 - F_{WR}(T_{WL}) \quad (15)$$

$F_{WR}(t_{WR})$ represents the cdf of the probability distribution (Gaussian/non-central F) [6]. P_{WF} obtained using (15) closely matches the result using Monte-Carlo simulations (Table-1).

3.5. Hold Stability Failure (H_F)

In the stand-by mode, the V_{DD} of the cell is reduced to lower the leakage power consumption. However, if the lowering of V_{DD} causes the data stored in the cell to be destroyed, then cell is said to have failed in the hold-mode [8] (Fig. 3c). Hence, for a hold-failure event, the minimum supply voltage that can be applied to the cell in the hold-mode (V_{DDHmin}), without destroying the data, is higher than the designed stand-by mode supply voltage (V_{HOLD}). Thus, the probability of hold-stability failure (P_{HF}) is given by:

$$P_{HF} = P\left[V_{DDHmin} > V_{HOLD}\right] \quad (16)$$

Lowering the V_{DD} of the cell (say V_{DDH} represents the cell V_{DD} at the hold mode) reduces the voltage at the node storing '1' (V_L in Fig. 1). Due to leakage of N_L, V_L will be less than V_{DDH} for low V_{DDH}.The hold-failure occurs if $V_L < V_{TRIP}$ of P_R-N_R. Hence, V_{DDHmin} can be obtained by solving:

$$V_L\left(V_{DDHmin}, \delta Vt_{PL}, \delta Vt_{NL}\right) = V_{TRIP}\left(V_{DDHmin}, \delta Vt_{PR}, \delta Vt_{NR}\right) \quad (17)$$

The estimated value of V_{DDHmin} closely follows the values obtained from MEDICI simulation (Fig. 8a). From (17), it is evident that V_{DDHmin} is a function of RVs δVt_{PL}, δVt_{NL}, δVt_{PR} and δVt_{NR}. The distribution of V_{DDHmin} ($f_{VDDHmin}(v_{DDHmin})$) can be approximated as a Gaussian one with mean and variance obtained using the procedure described in (6) (a non-central χ^2 distribution improves the accuracy for V_{DDHmin}s close to 0).(Fig. 8b). Hence, we can estimate P_{HF} as:

$$P_{HF} = \int_{V_{HOLD}}^{\infty} f_{VDDHmin}(v_{DDHmin})d(v_{DDHmin}) = 1 - F_{VDDHmin}(V_{HOLD}) \quad (18)$$

The P_{HF} obtained using (18) closely matches the result using Monte-Carlo simulations (Table-1).

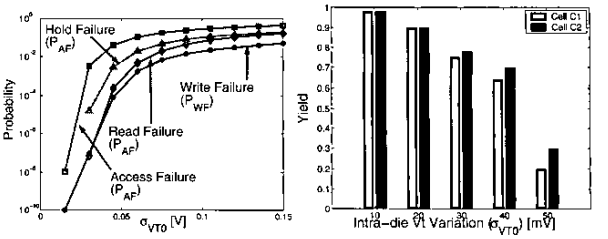


Fig. 9: Variation of failure Fig. 10: Variation of Yield with σ_{VT0}.

3.6. Estimation of Overall Failure Probability (P_F)

The overall failure probability is given by:

$$\begin{aligned} P_F &= P[Fail] = P\left[A_F + R_F + W_F + H_F\right] = P_{AF} + P_{RF} + P_{WF} + P_{HF} \\ &- P\left[A_F R_F\right] - P\left[A_F W_F\right] - P\left[A_F H_F\right] - P\left[R_F W_F\right] - P\left[R_F H_F\right] - P\left[W_F H_F\right] \\ &+ P\left[A_F R_F W_F\right] + P\left[A_F R_F H_F\right] + P\left[R_F W_F H_F\right] + P\left[W_F H_F A_F\right] - P[All] \end{aligned} \quad (19)$$

To simplify the estimations of the probabilities of the joint events, let us consider Table-II. It shows the direction in which δVt of different transistor has to move (δVt >0 or δVt<0) to cause each type of failures. For example, let us consider the joint event ($A_F R_F$). It can be observed that, among the four different ways of causing read-failure only δVt_{NR}>0 also causes the access failure. Hence, we argue that, $P[R_F A_F]$=(¼)min(P_{RF}, P_{AF}). The probabilities of other joint events can also be computed using similar arguments. We have also assumed that probabilities of simultaneous occurrence of more than two events are negligible (≈0). The estimated probabilities match the Monte-Carlo results very closely (Table-II). All of the different failure probabilities increase significantly with an increase in the sigma of Vt variation (using cell C1) (Fig. 9).

Table-II: Estimation of Probabilities of Joint Events

	δVt_{AXR}	δVt_{AXL}	δVt_{NR}	δVt_{NL}	δVt_{PR}	δVt_{PL}
R_F	$\delta Vt < 0$	NME*	$\delta Vt > 0$	$\delta Vt < 0$	NME	$\delta Vt > 0$
A_F	$\delta Vt > 0$	NME	$\delta Vt > 0$	NME	NME	NME
W_F	NME	$\delta Vt > 0$	$\delta Vt < 0$	NME	$\delta Vt > 0$	$\delta Vt < 0$
H_F	NME	NME	$\delta Vt > 0$	$\delta Vt < 0$	$\delta Vt < 0$	$\delta Vt > 0$
$P[A_F R_F]$=(¼)min(P_{RF}, P_{AF})			$P[R_F W_F]$=0		$P[R_F H_F]$= (¼)min(P_{RF},P_{HF})	
$P[A_F W_F]$=(¼)min(P_{AF},P_{WF})			$P[W_F H_F]$ = 0		$P[A_F H_F]$=(¼)min(P_{AF},P_{HF}	
*NME ≡ does Not have a Major Effect						

3.7. Estimation of Yield

To estimate the yield of memory, we define the failure probability of column (P_{COL}) (or row (P_{ROW})) as the probability that any of the cells (out of N cells) in that column (or row) fails. Assuming a column redundancy, the probability of failure of a memory chip (P_{MEM}) designed with N_{COL} number of columns and N_{RC} number of redundant columns, is defined as the probability that *more than* N_{RC} (i.e. at least N_{RC}+1) columns fail (similar definition is applicable for row redundancy). Hence, P_{COL} and P_{MEM} can be given by:

$$P_{COL} = 1 - (1 - P_F)^N \text{ and } P_{MEM} = \sum_{i=N_{RC}+1}^{N_{COL}} \binom{N_{COL}}{i} P_{COL}^{i} (1 - P_{COL})^{N_{COL}-i} \quad (20)$$

To estimate the yield, we have used Monte-Carlo simulations for *inter-die* distributions of L, W and Vt (assumed to be Gaussian).For each inter-die values of the parameters (say L_{INTER}, W_{INTER} and Vt_{INTER}) we estimate P_F, P_{COL} and P_{MEM} considering the intra-die distribution of δVt. Finally, the yield is defined as:

$$Yield = 1 - \left(\sum_{INTER} P_{MEM}\left(L_{INTER}, W_{INTER}, Vt_{INTER}\right) \Big/ N_{INTER} \right) \quad (21)$$

where, N_{INTER} is the total number of inter-die Monte-Carlo simulations (i.e. total number of chips). The yield decreases significantly with increasing σ_{VT0} (Fig. 10). In the estimation, we have assumed a standard deviation of 7% for inter-die distribution of L, W and Vt, N=32 cells, N_{COL}=512, N_{RC}=24, σ_{VT0}=30mV.

Table-I: Failure Probability Estimations for Different Cells (MonteCarlo / Estimation)

σ_{VT0}=80mV (A Large Value of σ_{VT0} is used to verify the results with Monte-Carlo Simulations of 10000 Vector) , V_{DD}=0.9V,V_{HOLD}=0.45V, T_{MAX}=75ps, T_{WL}=90ps)

Cells: C1≡(L_p= L_{npd}= L_{nax}=50nm, W_p=100nm, W_{npd}=200nm, W_{nax}=150nm); **C2≡**(L_p= L_{npd}= L_{nax}=50nm, W_p=150nm, W_{npd}=200nm, W_{nax}=150nm),

	P_{RF}	P_{AF}	P_{WF}	P_{HF}	$P[A_F R_F]$	$P[R_F W_F]$	$P[R_F H_F]$	$P[A_F W_F]$	$P[A_F H_F]$	$P[W_F H_F]$	$P[A_F R_F H_F]$	$P[A_F R_F H_F]$, $P[R_F W_F H_F]$, $P[W_F H_F A_F]$	P[All]	P_F
C1	0.041/0 .038	0.159/ 0.152	0.005/ 0.005	0.067/ 0.062	0.008/ 0.009	0/0	0.029/ 0.027	0/0.001	0.014/ 0.0155	0/0	0.002/0	0/0	0/0	0.223/ 0.21
C2	0.009/0 .008	0.150/ 0.152	0.028/ 0.022	0.029/ 0.031	0/0.002	0/0	0.008/ 0.006	0.007/ 0.005	0.006/ 0.008	0/0	0/0	0/0	0/0	0.221/ 0.192

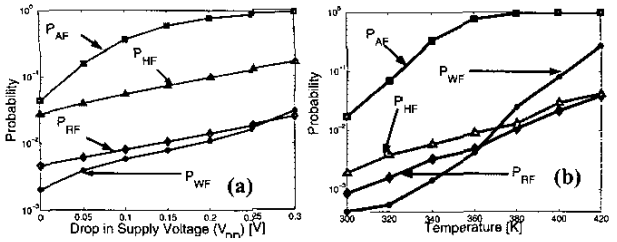


Fig. 11: Impact of (a) supply voltage drop and (b) temperature increase on the failure probability

4. DISCUSSIONS

4.1. Impact of Vdd and Temperature Variation

A drop in the supply voltage increases the cell failure probabilities. (Fig. 11a). The impact of supply voltage drop is most significant for the access time failure. The derived model can also be extended to include Vdd of a cell as an independent Gaussian random variable. Fig. 11b shows that the failure probabilities increase with an increase in the temperature. The impacts of temperature increase is more severe on the access time and write failure because of (a) reduction in the ON current of the access transistors and (b) increase in the junction capacitances.

4.2. Transistor Size and Cell Failure Probability

The length and width of different transistors of the cell (i.e. L_{nax}, W_{nax}, L_{npd}, W_{npd}, L_{pup}, W_{pup},) impact the cell failure probability principally by modifying: (a) the nominal values of T_{ACCESS}, V_{TRIP} & V_{READ}, T_{WRITE} and V_{DDHmin}, (b) the rate of change of these parameters with Vt variation thereby changing the mean and the variance of these parameters, and (c) the variance of the Vt variation (see (1)). For example, Fig. 12 shows that, along with the nominal value, the mean and the standard deviation of T_{ACCESS} significantly vary with W_{npd} and W_{nax}. In this section, we study the impact of variation of strength of different transistors (only width is used to vary the strength) on the cell failure probability. Variation of the strength using channel length follows the same trend.

Fig. 13 shows that, a weak access transistor (small W_{nax}) reduces P_{RF} (V_{READ} decreases). However, it increases P_{AF} (increases η and σ of T_{ACCESS} (Fig. 12)) and P_{WF} (Fig. 13) and has very small impact on P_{HF}. Reducing the strength of the PMOS pull-up transistors (by decreasing W_p) reduces P_{WF} (reducing I_{dsPL}), but increases P_{RF} (lowers V_{TRIPRD}). P_{AF} does not depend strongly on PMOS strength (Fig. 13). P_{HF} improves with an increase in W_p as the node L is more strongly coupled to the supply voltage ($V_L \rightarrow V_{DDH}$). Increasing W_{npd} increases the strength of pull-down NMOSs (N_L & N_R)). This reduces P_{RF} ($V_{READ} \downarrow$) and P_{AF} by increasing the strength of N_R (Fig. 13). Increase in width of N_R has little impact on P_{WF}. Although, it slightly increases the nominal value of T_{WRITE}, the reduction of σ_{VT} of N_R (see (1)) tends to reduce σ_{TWRITE} and hence P_{WF} remains almost constant. An increase in the V_{TRIP} of P_R-N_R initially reduces P_{HF} with the increase in W_{npd}. However, a higher width of N_L reduces V_L (from the applied V_{DDH}) due to an increase the leakage of N_L. Consequently, a very high W_{npd} increases the P_{HF}. Due to the variation in the failure probability, the choice of the transistor sizes has a strong impact on the yield (Fig. 14a). Hence, it can be concluded that, a statistical approach to the design of the transistor sizes is necessary to maximize the yield. The derived failure probability models can be effectively used for such statistical optimizations.

4.3. Memory Architecture and Yield

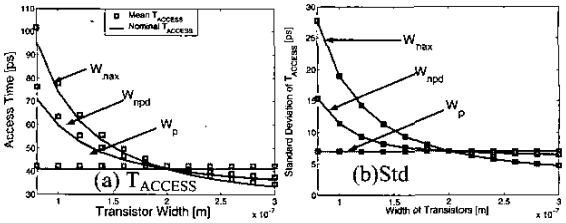


Fig. 12: The impact of transistor size on the distributions of T_{ACCESS}

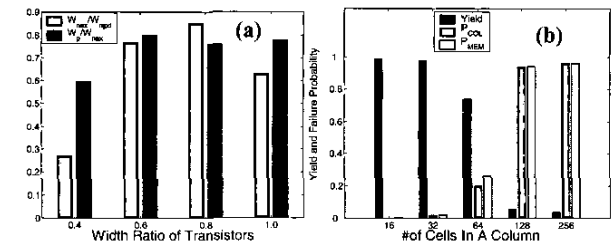


Fig. 14: Impact of (a) circuit (transistor size) and (b) architecture (#of row (column length) and #of columns) on yield. In (b) transistor sizes were chosen to maximize yield following (a). (σ_{VT0}=20mV)

Increasing the number of cells in a column (column length or #of rows) increases the cell failure probability (particularly P_{AF} as C_{BL} and I_{BL} increases in (5) resulting in higher T_{ACCESS}). Moreover, P_{COL} and hence P_{MEM}, increases significantly with the column length (see (20)). However, for a constant memory size, increasing column length reduces the number of columns, which tends to reduce P_{MEM} (assuming a constant redundancy). Consequently, to maximize the yield, the design of the memory organization has to consider its impact on the failure probabilities. Fig. 14b shows the variation column failure probability, the memory failure probability and yield of a 2KB cache with the column length (# of redundant column kept constant). It can be observed that, yield strongly depends on the column length.

5. CONCLUSION

In this work, we have proposed a semi-analytical method to estimate the failure probability of an SRAM cell due to parameter variation. The derived models have been used to predict the yield of memory at an early stage of design. The proposed models provide a statistical approach for optimizing the memory design, which is necessary for maximizing yield in nano-meter regime.

Acknowledgement: We thankfully acknowledge many helpful discussions with Dr. Dinesh Somasekhar of Intel Corp.

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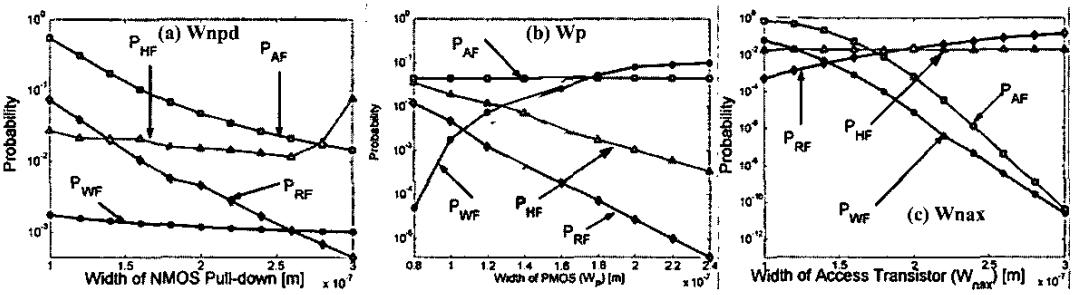

Fig. 13: Variation of Cell Failure Probabilities with Cell structure