Data-Retention Flip-Flops for Power-Down Applications

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Abstract

A novel technique for retaining data in flip-flops in power-down applications is presented. In flip-flops data is stored in cross-coupled inverters. Cross-coupled inverters can hold their states in the power down mode, if their inputs are properly gated. Based on this fact, simple clock and data gating circuitries are employed in flip-flops to retain their data in the power-down mode without using any extra data-preserving latches. In a predictive 70nm technology node, a transmission-gate flip-flop based on the proposed data-retention scheme exhibits 18X reduction in standby leakage compared to a conventional transmission-gate flip-flop. The proposed data-retention scheme also exhibits 40% area reduction compared to the conventional balloon scheme. A 16-bit shift-register using data-retention flip-flops has been successfully fabricated and tested in a 0.25μm CMOS process.

1. Introduction

To achieve higher density and performance and lower power consumption, CMOS technology has been scaled down for several decades. Supply voltage (V_{DD}) has been scaled down in order to keep the power consumption under control. Hence, the transistor threshold voltage (V_{th}) has to be commensurately scaled to maintain a high drive current and achieve performance improvement. However, the threshold voltage scaling results in the substantial increase of the subthreshold leakage current [1]. Therefore, as a result of technology scaling, leakage power is becoming a major contributor to total power consumption.

Leakage current is present in both active and standby modes of operation. In order to reduce the standby leakage power consumption, circuits can be put in the power-down mode by switching-off the power during the standby mode [2]. The power can be switched-off by switching-off either the supply voltage (V_{DD}) or ground (GND) of the circuit. The transistors switching-off the power are called sleep transistors. For switching-off the V_{DD} (gated-V_{DD}), PMOS sleep transistors are required between the real V_{DD} and virtual V_{DD} of the circuit. However, for switching-off the GND (gated-GND), NMOS sleep transistors are used between the real GND and virtual GND of the circuit. Since the sleep transistors are fairly large, gated-GND is preferred to gated-V_{DD} because the NMOS sleep transistors can be much smaller than the PMOS sleep transistors.

The state of a circuit which is stored in flip-flops may be lost in the power-down mode. Therefore, in power-down applications where the state of the circuit is required to be preserved, shadow or balloon latches, that state of the circuit during the power-down mode [2]. Conventional data-retention scheme based on the balloon latch is shown in Fig. 1 [2]. The power-down scheme shown in Fig. 1(a) uses the gated-GND scheme. Fig. 1(b) shows a balloon data-retention scheme applied to a Transmission Gate Flip-Flop (TGFF). As shown in Fig. 1(b), the balloon latch and some switches which are not in the critical paths use high threshold voltage (high-V_{th}) transistors to reduce their leakage power, since they are always powered. This conventional scheme requires extra data-preserving latches (balloon latches) and complicated timing for transferring data back and forth between balloon latches and flip-flops on any transition from power-down to active mode and vice versa. To overcome these problems, several data-retention schemes have been proposed for power-down applications [2-6]. However, in some of the previous techniques, depending on the internal state of flip-flops in the power-down mode, there can be sneak leakage paths due to interaction between gates which are always powered and gates which are powered down [6]. In [6], leakage feedback flip-flop has been proposed that eliminates all possible sneak leakage paths during the power-down

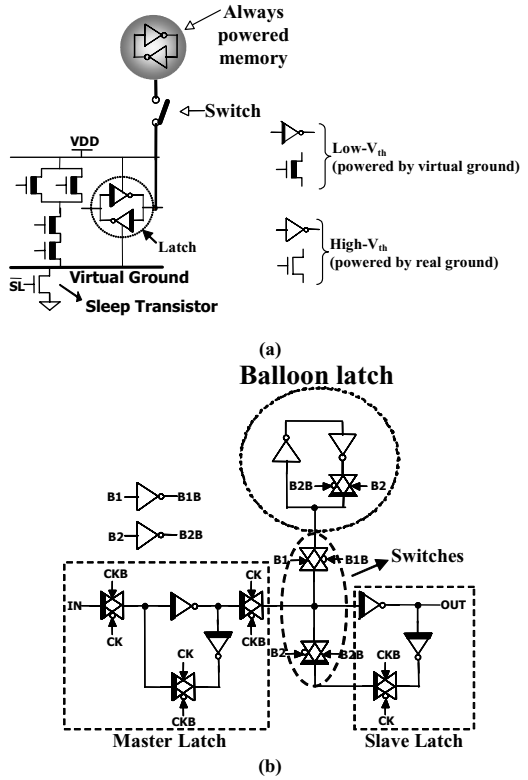

Fig. 1. (a) Conventional data-retention scheme (b) balloon latch applied to a transmission-gate flip-flop

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mode. However, this technique uses several local sleep transistors and helper sleep transistors of both polarities (NMOS and PMOS) for each flip-flop, incurring considerable area overhead. Although the helper sleep transistors are in non-critical paths to avoid any performance penalty, however, due to their significant gate capacitance, they result in power overhead as well.

We propose data-retention flip-flops that preserve their states in the power-down mode without using any extra data-preserving latches or control signals. Moreover, our scheme can retain data with a single polarity sleep transistor. Our scheme does not require any local or extra sleep transistor, showing no performance, power, or area penalty. Moreover, since our scheme does not use any constantly powered gates in data paths, there are no sneak leakage paths in the power down mode.

2. Data-Retention Flip-Flop (DRFF)

In flip-flops, data is stored in cross-coupled inverters. For example, in the Transmission-Gate Flip-Flop (TGFF) of Fig. 1(b), the two inverters in the master and slave latches form cross-coupled inverters to hold the data. For writing data to the flip-flop, the switch (transmission-gate) interfacing the input data to the cross-coupled inverter is turned-on. For holding the written data, the interfacing switch is turned-off and another switch is turned-on to put the inverters in a cross-coupled loop. The cross-coupled inverters can retain their data even in the power-down mode. Based on this fact, Fig. 2 shows our proposed data-retention scheme for flip-flops. However, the clock and data inputs may change the data stored in the flip-flop. Therefore, the data and clock paths to the cross-coupled inverters are switched-off in the power-down mode to prevent them from destroying the data stored in the cross-coupled inverters. Hence, the internal clock and

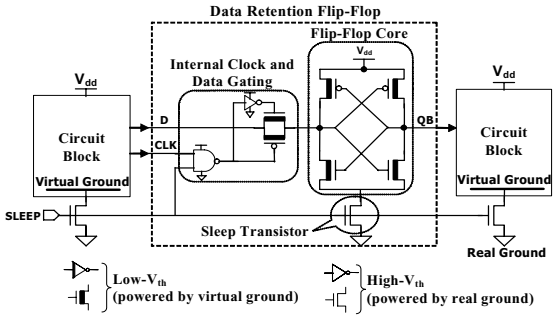

Fig. 2. Proposed data-retention scheme

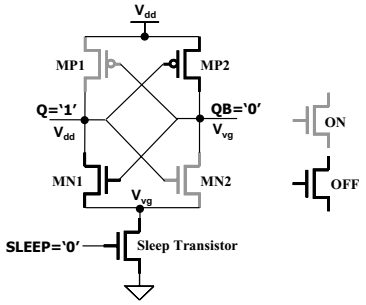

Fig. 3. Cross-coupled inverters in sleep mode

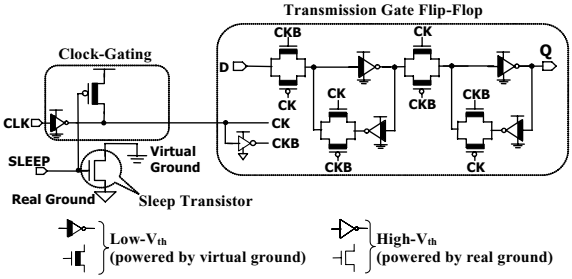

Fig. 4. Data-retention transmission-gate flip-flop

data gating circuitry needs to be always powered. The internal gating circuitry is implemented using high-V_{th} transistors to minimize the standby leakage. However, as it will be shown, in actual flip-flop designs, only one inverter needs to be always powered. The sleep signal switches-off the ground of the circuit and also gates the clock and data inputs of the flip-flop. It should be noted that the sleep transistor may be shared among a group of flip-flops.

To better describe the data-retention property, Fig. 3 shows the cross-coupled inverters in the sleep mode when the node Q is at logic level '1' and QB is at logic level '0'. In the sleep (power-down) mode, the sleep transistor is OFF and the voltage of the virtual ground node is determined by the leakage balance between the cross-coupled inverter and the sleep transistor. By properly sizing the sleep transistor, this voltage can be low enough such that the data stored in the cross-coupled inverter is retained. In Fig. 3, the voltage of output QB, which is at low logic level, is same as the voltage of the virtual ground (V_{vg}), since transistor MN2 is ON. Therefore, the transistor MN1 remains OFF since its gate and source have the same voltage of V_{vg}. By properly sizing the sleep transistor, the voltage V_{vg} can be small enough to keep the transistor MP1 ON, and therefore, the output Q at voltage V_{dd}. When the circuit returns to the active mode, the sleep transistor turns-on and pulls down the virtual ground voltage (V_{vg}) to zero, restoring the data stored in the cross-coupled inverters.

Fig. 4 shows the detailed schematic of a Transmission-Gate Flip-Flop (TGFF) based on the proposed data-retention scheme. The internal clock and data gating circuitry is only composed of one inverter and one PMOS transistor. The inverter of the clock-gating circuitry may not be required if the clock is already buffered through the clock distribution network. In the sleep mode, the PMOS transistor pulls up the clock input node of the flip-flop to V_{DD}. Therefore, the data input is also automatically gated by the transmission gate at the input of the flip-flop. Moreover, the loop of the cross-coupled inverters in the master latch is closed to retain the data stored in the master latch. In this scheme only the inverter that generates signal CKB is required to be always powered, and therefore, can be implemented using high-V_{th} transistors.

The data-retention TGFF (DR-TGFF) (Fig. 4) and the balloon-TGFF (Fig. 1(b)) are designed in the 70nm CMOS technology node, using Berkeley Predictive

Technology Models [7]. The TGFF without any sleep transistor or data-retention circuitry and with all low-V_{th} transistors is also designed for comparison. Comparisons of standby leakage current in active and power-down (sleep) modes at different supply voltages are shown in Fig. 5. In Fig. 5, "original TGFF" represents the TGFF without any sleep transistor or data-retention circuitry. In the active mode, the DR-TGFF shows minimum leakage. Compared to the original TGFF, the DR-TGFF exhibits 18X leakage reduction in the power-down mode. The flip-flop characteristics are summarized in Table 1. Our technique exhibits improvements in leakage and total power and power-delay-product (PDP) compared to the conventional balloon scheme. Moreover, since our technique does not need extra latches for data-retention, 40% area and transistor-count reduction is achieved compared to the conventional balloon scheme.

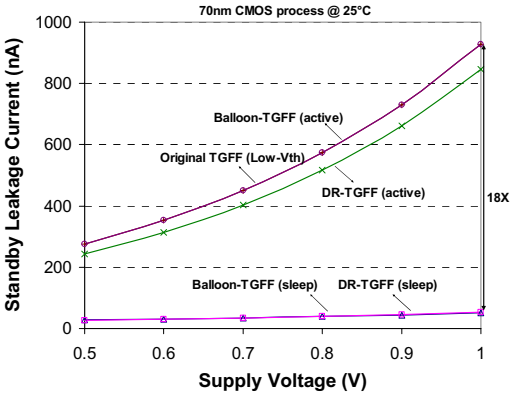

Fig. 5. Standby leakage comparisons

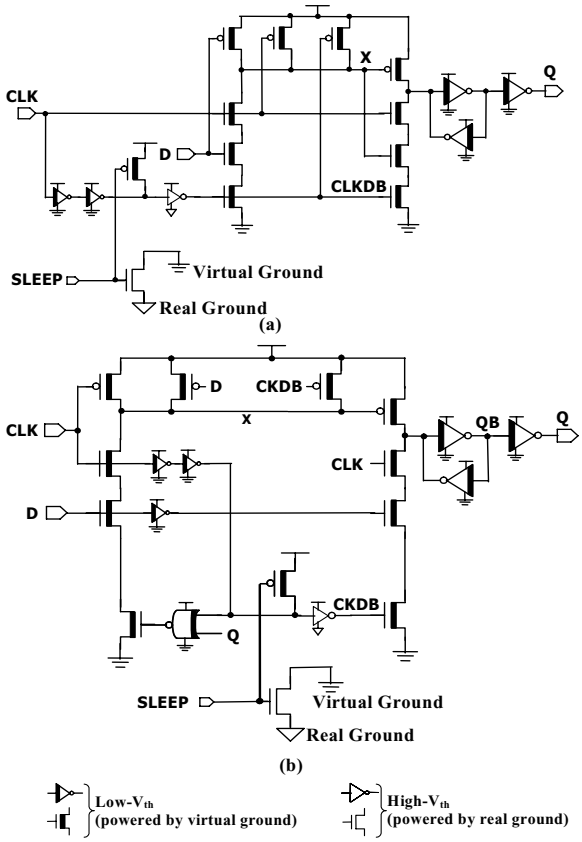

Fig. 6. Dynamic flip-flops with data-retention feature: (a) Hybrid Latch Flip-Flop (b) Conditional Capture Flip-Flop

The proposed scheme can be applied to dynamic flip-flops as well. Fig. 6 shows a Hybrid Latch Flip-Flop (HLFF) [8] and a Conditional Capture Flip-Flop (CCFF) [9] with the data-retention feature. In these flip-flops, the data-retention overhead is only one PMOS transistor for clock gating; and only one inverter is required to be high-V_{th} (always powered). In these flip-flops, the high-V_{th} inverter is not in the critical path of the flip-flop and therefore, does not impose any delay penalty on the flip-flop.

3. Shift-Register with DRFFs

To demonstrate the effectiveness of the proposed data-retention scheme, we have implemented a 16-bit shift-register fabricated in a 0.25µm CMOS process. Fig. 7(a) shows the schematic diagram of the 16-bit shift-register using data-retention TGFFs (Fig. 4). There are two sleep transistor shared by the circuit. In this design, the clock gating circuitry (clock inverter and PMOS transistor in Fig. 4) is shared among each group of four flip-flops to further reduce the data-retention overhead. The SLEEP input is sampled by a flip-flop, which is always powered, to synchronize the internal sleep signal with the clock signal. The NOR gate performs clock-gating in the power-down mode. The power-down timing of the circuit is shown in Fig. 7(b). At the first rising edge of CLK when SLEEP is high, the internal sleep signal switches to low, putting the circuit in the power-down mode. At the first rising edge of CLK when SLEEP returns to low, the internal sleep signal returns to high, putting the circuit in the active mode and restoring data stored in flip-flops. Fig. 8 shows simulation waveforms of the data-retention shift-register. The supply voltage is 2.5V; and the voltage of the virtual ground saturates to 550mV in the power-down mode.

The design was fabricated in a 0.25µm CMOS technology as shown in Fig. 9. The functionality of the fabricated design in both the power-down and active modes has been verified by measurements.

Table 1. Flip-flop characteristics
(70nm CMOS; 25°C; VDD=1V; Clock frequency=200MHz; Data switching activity=100%)

Flip-Flop	Transistor count	Area (μm^2)	CLK-Q delay (pS)	Total power in active mode (µW)	PDP (fJ)	Standby leakage in sleep mode (nA)	Standby leakage in active mode (nA)
Balloon	32	98	38.17	4.37	0.167	927.61	52.46
DRFF	19	59	39.54	4.16	0.164	846.67	50.39
DRFF improvement over Balloon	41%	40%	-4%	5%	2%	9%	4%

4. Conclusion

A novel data-retention scheme for power-down applications and applicable to different types of flip-flops is proposed. The proposed data-retention flip-flops need no extra data preserving latches, and therefore impose minimal area, power, and delay penalties for data-retention. The effectiveness of the proposed scheme was demonstrated by design and fabrication of a 16-bit data-retention shift-register.

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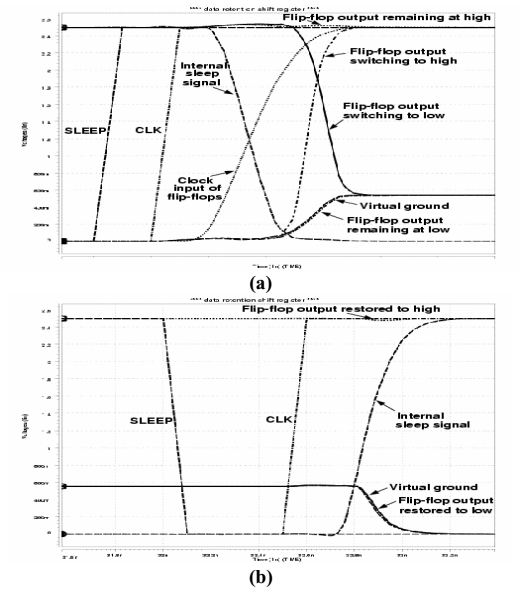

Fig 8. HSPICE Simulation waveforms of the shift-register (a) transition to power-down mode (b) transition to active mode

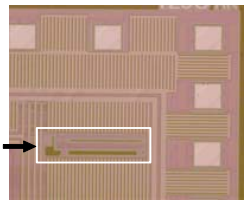

Fig. 9. Microphotograph of data-retention shift-register

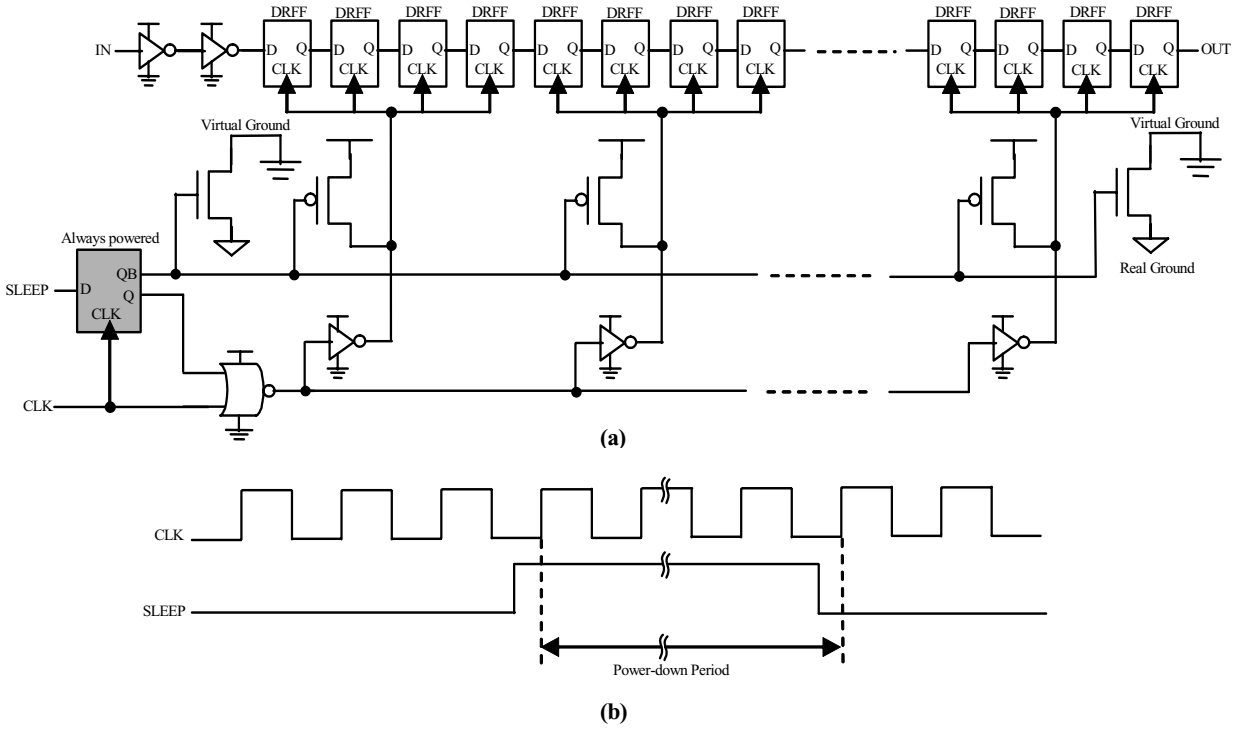

Fig. 7. (a) Schematic diagram of 16-bit shift-register using data-retention flip-flops (b) power-down timing