Dual-Edge Triggered Level Converting Flip-Flops

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Abstract

Level converting flip-flops are critical elements in dual-V_{DD} design for level conversion at the interface from low supply to high supply regions. Level converting flip-flops also provide energy savings on the clock distribution network by using low-swing clock signals. We propose dual-edge triggered level converting flip-flops that provide data sampling and level converting functions at both rising and falling edges of a low-swing clock. Adding the dual-edge triggering feature to level converting flip-flops, the clock frequency can be reduced by half, resulting in 50% power savings on the clock tree in addition to the savings due to low voltage swing clock. Moreover, the proposed flip-flops outperform the existing level converting flip-flops in terms of performance. The dual-edge triggering capability is achieved by using a dual pulse clock generator that generates short pulses at both rising and falling edges of the clock. Based on simulation results in a 0.25μm CMOS technology, the proposed flip-flops exhibit up to 68% delay reduction as compared to existing level converting flip-flops.

1. Introduction

Multiple supply voltage (V_{DD}) design technique can be very effective in reducing power consumption of CMOS circuits without sacrificing system performance [1]. Since the speed requirements of the non-critical paths are lower than the critical paths, supply voltage of non-critical paths can be lowered without degrading system performance. Whenever an output from a low V_{DD} (V_{DDL}) region has to drive an input to a high V_{DD} (V_{DDH}) region, a level conversion is needed at the interface. To reduce the overhead of the level conversion, low V_{DD} regions are followed by pipeline flip-flops and the level conversion is merged into the flip-flops [1]. The flip-flops simultaneously perform latching and level shifting and are called level converting flip-flops. The performance and power consumption of the level converting flip-flops are critical to the effectiveness of the multiple V_{DD} schemes. The clock and data inputs of a level converting flip-flop have low voltage swing of V_{DDL} and the output has high voltage swing of V_{DDH}.

The level converter can be merged to the slave part of a master slave flip-flop, which results in the Slave Latch Level Shifting (SLLS) flip-flop proposed in [1] and shown in figure 1-a. The master latch operates with the low supply (V_{DDL}) and the level converter is powered by the high supply (V_{DDH}). This scheme suffers from long delay, especially when V_{DDL} is very low compared to V_{DDH}. To reduce this delay overhead, new level converting flip-flops have been proposed recently, as shown in Fig. 1-b to 1-d [2,3]. These flip-flops are pulsed and are faster than master slave flip-flops. The Self-Precharging Flip-Flop (SPFF), Fig. 1-b, employs a self-precharching technique to precharge its dynamic node and does not require the clock signal to drive PMOS precharging transistors [2]. The self-precharging circuit automatically returns the flip-flop to the precharge mode after enough time has been allowed for the input data to propagate and get latched to the output. The Pulsed-Precharged (PPR) flip-flop, Fig. 1-d, is similar to SPFF; however, the precharging operation is started by an NMOS precharging transistor and completed by the inverter loop controlled by the clock signal [3]. SPFF and PPR flip-flops also incorporate the conditional capturing technique to remove redundant internal transitions when input data is calm. The Pulsed Half-Latch (PHL), Fig. 1-c, uses an explicit pulse generator that generates pulses at rising edges of the clock to capture the data to a half-latch level converter [3]. The pulse generator can be shared among a group of flip-flops to reduce the power and area overhead of pulse generation.

The major fraction of the total power in highly synchronous systems, such as microprocessors, is dissipated over the clock tree [4]. The level converting flip-flops provide energy savings on the clock tree by enabling the use low voltage swing clock signals. Dual-edge triggering is also another technique that has been incorporated into flip-flops for significant clock power reduction [5,6]. Dual-edge triggering feature in flip-flops helps to reduce the clock frequency by 50%, thereby saving energy on the clock distribution network [6].

The existing level converting flip-flops cannot operate on dual-edge and the existing dual-edge triggered flip-flops are not capable of level-conversion. Therefore, we propose Dual-Edge Triggered Level-Converting Flip-Flops (DETLCFF) that provide both dual-edge triggering and level-converting features.

2. Dual-Edge Triggered Level Converting Flip-Flops

The proposed dual-edge triggered level converting flip-flops are pulsed flip-flops. Therefore, a dual pulse clock generator is needed to generate pulses at both rising and falling edges of a low-swing clock. Fig. 2 shows such a dual pulse generator, which is a self-precharged dynamic gate. The low swing clock and its inverted and delayed versions are ANDed and then ORed in the evaluation network of the dynamic gate. The low-swing

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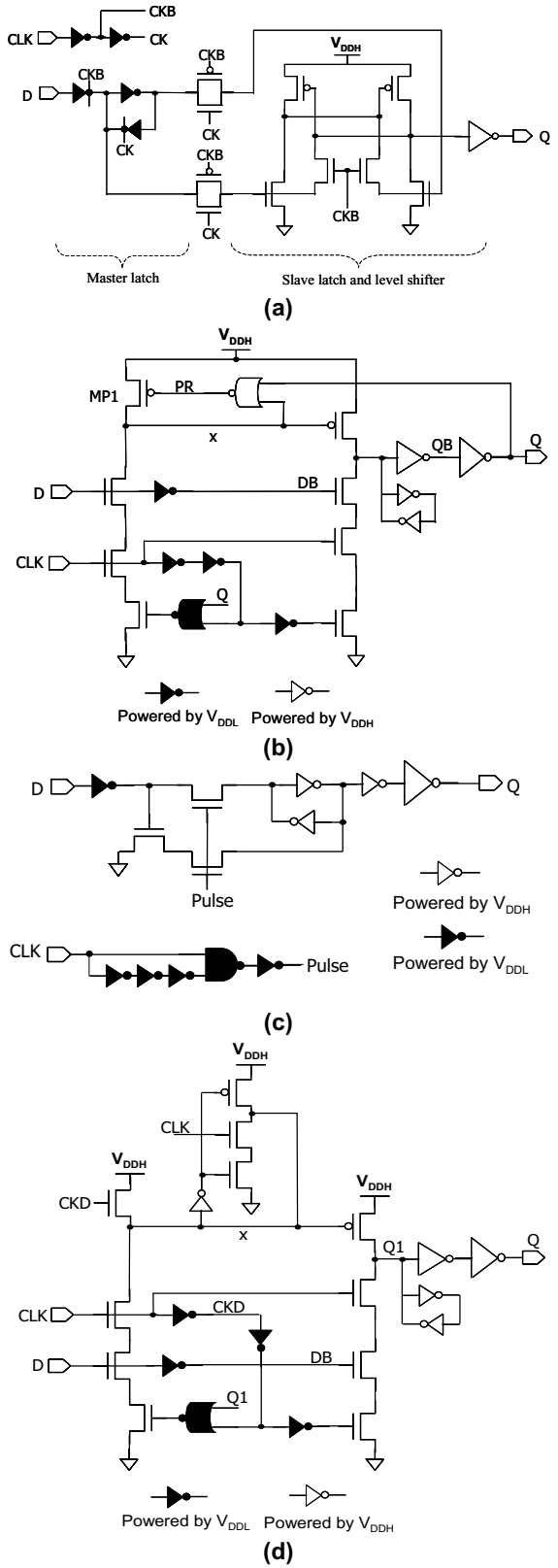


Fig. 1. Existing Level Converting Flip-Flops (LCFF): **(a)** Slave Latch Level Shifting (SLLS) **(b)** Self-Precharging Flip-Flop (SPFF) **(c)** Pulsed Half-Latch (PHL) **(d)** Pulsed Precharged (PPR)

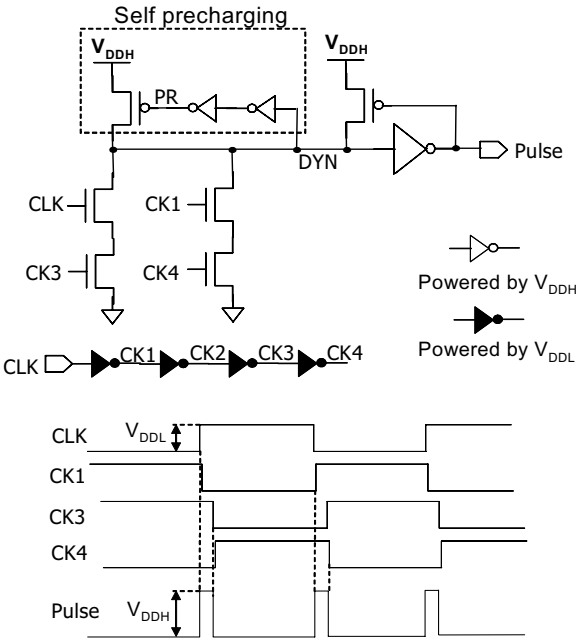


Fig. 2. Proposed Dual Pulse Generator

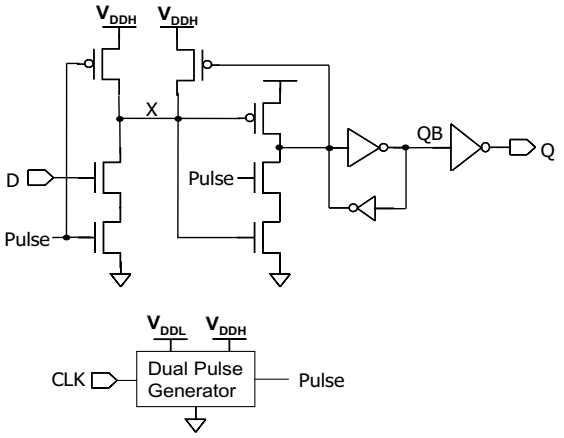


Fig. 3. Proposed Dynamic Dual-Edge Triggered LCFF

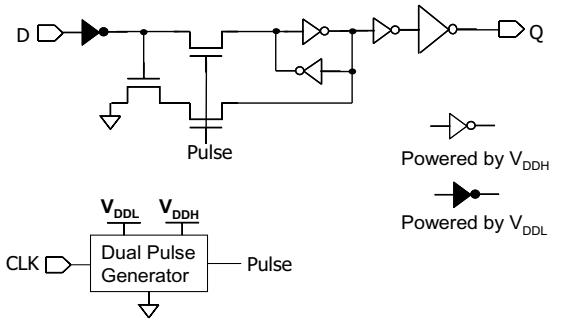


Fig. 4. Proposed Static Dual-Edge Triggered LCFF

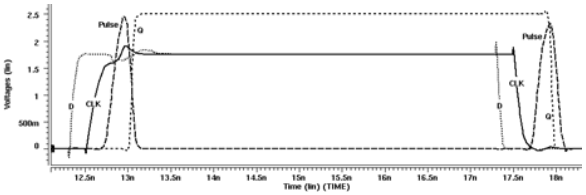


Fig. 5. Typical simulation waveforms of DETLCFF

clock signals drive only NMOS transistors in the dynamic gate, preventing any short circuit current. The generated pulse is a full-swing signal which is helpful for improving performance of the proposed flip-flops. The level conversion occurs on the dynamic node (DYN), which is precharged to V_{DDH} by the self precharging circuit. If any discharge occurs on the dynamic node, the PR node also switches to low after some delay through the inverters; and the prechargimg PMOS transistor recharges the dynamic node to V_{DDH}. The pulse duration can therefore be easily adjusted by the delay of the self precharging circuit. Another benefit of the self-precharging technique is that it reduces the clock load and saves clock power. After precharging is over, the precharing transistor is turned off and the dynamic node is kept charged by the keeper transistor and the circuit is ready for pulse generation at the next clock edge. The pulse generator can be shared among a group of flip-flops to reduce its power and area overhead.

Fig. 3 shows the schematic of the first proposed dual-edge triggered level converting flip-flop. It is a dynamic flip-flop with the precharge node (X) precharged to V_{DDH} by the full-swing pulse generated by the dual pulse generator. When the pulse arrives, the result of the evaluation of the input data is captured into the output latch (cross-coupled inverters). The input data is a low-swing signal and only drives an NMOS transistor. The order of the transistor stack in the sampling path is based on the arrival time of the signals. The data input, which is the latest arriving signal, drives the transistor closest to the dynamic node. This ordering increases the performance of the flip-flop and allows for more negative setup time. Negative setup time provides soft clock edge [7], and is powerful in eliminating clock skew and jitter from timing budget in critical paths. A small keeper transistor prevents the dynamic node (X) from becoming floated if input (D) is low during the presence of the pulse. The dynamic operation and full-swing pulse result in the best performance for this flip-flop, making it suitable for critical paths.

Fig. 4 shows the second proposed dual-edge triggered level converting flip-flop which is a dual-pulsed static flip-flop. This flip-flop is similar to the PHL level converting flip-flop; however, it uses the dual-pulse generator (Fig. 2) to capture the low-swing input data into a latch at both rising and falling edges of the clock. The latch which is cross-coupled inverters supplied by high V_{DD} provides level conversion as well. The static operation results in less power consumption at the cost of lower performance as compared to the dynamic flip-flop. Lower power consumption makes this flip-flop suitable for uncritical paths.

Fig. 5 shows the typical waveforms of the proposed flip-flops, which are obtained by HSPICE simulations of the flip-flops using typical models of a 0.25µm CMOS technology at 25°C with V_{DDH}=2.5V and V_{DDL}=1.75V.

3. Simulation results and comparisons

The delay metric for flip-flops is minimum data to output (D-to-Q) delay, which includes both setup time and clock to output (CLK-to-Q) delay [8]. The existing single-edge triggered level converting flip-flops and the proposed dual-edge triggered level converting flip flops are designed and optimized in a 0.25µm CMOS technology. For non-critical transistors, minimum sizes were used and critical transistors were optimized to minimize the power delay product of the flip-flops. The optimizations were done at V_{DDH}=2.5V, V_{DDL}=0.7×V_{DDH}=1.75V, 25°C, output load of 30fF, data switching activity of 50%, and clock frequency of 200MHz for the single edge-triggered flip-flops, and clock frequency of 100MHz for the dual-edge triggered flip-flops. The power dissipation due to switching of output capacitance was excluded to get the net power dissipation in the flip-flops. Then V_{DDL} was swept from

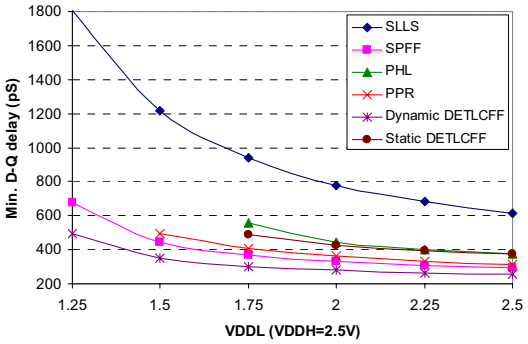
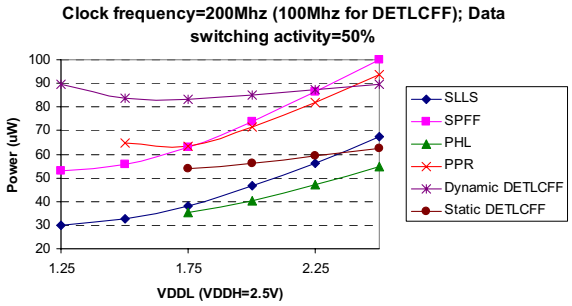
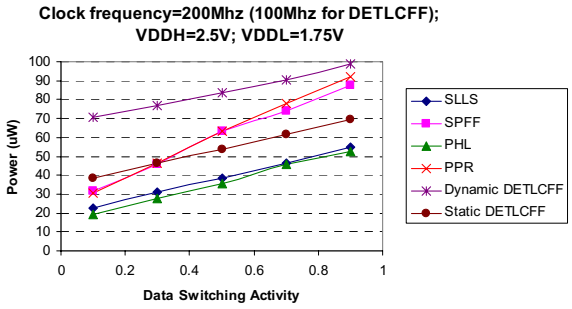


Fig. 6. Delay versus V_{DDL}



(a)



(b)

Fig. 7. Power comparisons **(a)** power versus V_{DDL} **(b)** power versus data switching activity

Table 1. Flip-flop characteristics (VDDH=2.5V ; VDDL=1.75V ; Output load=30fF ; Clock frequency=200MHz (100MHz for DETLCFF); Data switching activity=50%)

Flip-Flop	Transistor count	Total transistor width (μm)	Setup time (pS)	Min. D-Q delay (pS)	Power (μW)	PDP (fJ)	PDP Ratio
SLLS	26	22.9	298	938	38.3	35.9	1
SPFF	32	37.3	-53	372	63.1	23.5	0.65
PHL	16	19.3	-8	560	35.6	19.9	0.55
PPR	33	39.2	-14	407	63.6	25.9	0.72
Dynamic DETLCFF	20	30.1	-296	300	83.4	25	0.7
Static DETLCFF	18	23	-45	491	53.9	26.4	0.74

V_{DDH}=2.5V down to 0.5×V_{DDH}=1.25V and power and delay of the flip-flops were measured. For the proposed and PHL flip-flops which have explicit pulse generator, the pulse generator was shared among a group of four flip-flops. The power of the pulse generator was therefore divided by four and added to the power of a single flip-flop to get the total power for pulsed flip-flops. Fig. 6 shows delay comparisons of the flip-flops at different V_{DDL} voltages. As observed from Fig. 6, the proposed dynamic DETLCFF shows the best performance for all V_{DDL} voltages, making it suitable for critical paths. The performance improvement mainly attributes to the dynamic nature of the flip-flop and the full-swing pulse. As observed from Fig. 6, the dynamic flip-flops show smaller delays as compared to static flip-flops. SPFF has the best delay among the single-edge triggered level converting flip-flops. The static DETLCFF has a performance similar to the PHL flip-flop which is much better than that of the conventional SLLS flip-flop. However, they fail to operate at V_{DDL} below 1.75V, because the low voltage input inverter fails to change the state of the latch (cross-coupled inverters) supplied by the high V_{DD}. PPR failed to operate at V_{DDL} below 1.5V because of failure in the precharging operation which is initiated by an NMOS precharging transistor. Dynamic DETLCFF and SPFF can operate at smaller V_{DDL} voltages. Fig. 7 shows power comparisons of the flip-flops at different V_{DDL} and different switching activities. As observed from Fig. 7, the dynamic flip-flops show more power than the static flip-flops. Dynamic DETLCFF typically shows more power consumption except at large V_{DDL} values. The static DETLCFF, however, shows smaller power consumption and is comparable to that of SLLS and PHL. Therefore, static DETLCFF is more suitable for non-critical paths.

Table 1 shows numerical results for different flip-flops. Dynamic DETLCFF shows the smallest delay which is 68% less than that of the SLLS. It also shows an improvement of 30% in Power-Delay Product (PDP). The static DETLCFF shows less power consumption than that of the dynamic DETLCFF, making it more suitable for non-critical paths. Although PHL flip-flop has the smallest power consumption; however, by using the DETLCFF's, and therefore operating at half the clock frequency, an additional 50% savings on the clock tree power, which is a significant fraction of total chip power, can be achieved. The areas of the proposed flip-flops (represented by total number of transistors and total transistor width) are fairly small compared to those of SPFF and PPR. Operating at half the clock frequency, the proposed dual-edge triggered flip-flops show smaller power dissipation associated with the clock input capacitance. Moreover, operating at half the clock frequency reduces the power dissipation over the clock tree by 50%. In terms of setup time, the proposed flip-flops provide significant negative setup time which is very useful for clock skew tolerance and time borrowing in critical paths.

4. Conclusion

We propose dual-edge triggered level-converting flip-flops that offer both level converting and dual-edge triggering features. The proposed flip-flops provide significant energy savings on the clock network by both lowering the clock voltage swing and halving the clock frequency. Moreover, the dynamic dual-edge triggered level converting flip-flop outperforms existing single-edge triggered level converting flip-flops in terms of performance and is therefore well suited for level conversion in critical paths in multiple-supply voltage designs.

5. References

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