ICM 2003, Dec. 9-11, Cairo, Egypt.

Comparative Energy and Delay of Energy Recovery and Square Wave Clock Flip-Flops for High-Performance and Low-Power Applications

Aliakbar Ghadiri[1] and Hamid Mahmoodi-Meimand[2]
[1]Department of Electrical Engineering, Iran University of Science and Technology, Narmak, Tehran 16844, Iran
[2] School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA
ghadiri@iust.ac.ir mahmoodi@ecn.purdue.edu

Abstract

Flip-flops are essential elements of a design from both delay and energy aspects. A significant fraction of the total power in highly synchronous systems is dissipated over clock networks. Hence, low-power clocking schemes are promising approaches for future designs. Recently, there has been published several energy recovery flip-flops that enable energy recovery from the clock network, resulting in significant energy savings. However, there has not been shown any extensive power and delay comparison between energy-recovery and square clock flip-flops. We compare the energy recovery flip-flops with square wave clock flip-flops in terms of power, delay, and area. Based on the simulation results using BPTM 0.18μm CMOS technology, at a frequency of 200MHz, the differential energy recovery flip-flops exhibit more than 14% delay reduction and power reduction of more than 43% compared to the differential square-wave clock flip-flops. The single-ended energy recovery flip-flops show more than 22% delay reduction and power reduction of more than 16% compared to the single-ended square wave clock flip-flops.

Keywords: energy-recovery, flip-flop, low-power, square-wave clock

1. Introduction

The major fraction of total power in synchronous digital systems is dissipated over the clock distribution network. For example, in the Itanium™ microprocessor, more than 30% of the total chip power is due to the clock distribution network [1]. Thus, innovative clocking techniques for decreasing the power consumption of the clock networks are required for future designs.

Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an AC-type (oscillating) supply voltage [2]. Since the clock signal is typically the most capacitive signal, applying energy recovery techniques to the clock network recycles the energy from this capacitance in each cycle of the clock. However, for this technique to work effectively there is a need for energy recovery flip-flops that can operate with a sinusoidal clock. Recently, there has been published several energy-recovery flip-flops that work effectively with a single phase sinusoidal clock [8]. However, there has not been shown any extensive power and delay comparison between energy-recovery and square-wave clock flip-flops. In this paper, we show an extensive comparison between the energy recovery flip-flops and square-wave clock flip-flops in terms of delay, power, and area. Based on our results, the energy recovery flip-flops exhibit significant reduction in delay, power, and area as compared to the square wave-clock flip-flops.

The remainder of this paper is organized as follows. In sections 2 and 3, the square-wave clock flip-flops and the energy recovery flip-flops are reviewed. In section 4, extensive simulation results of individual flip-flops and their comparisons are presented. Finally, the conclusion of the paper appears in Section 5.

2. Square-wave clock flip-flops

Fig. 1 shows the schematic diagram of representative high performance square wave clock flip-flops. They are Transmission-Gate Flip-Flop (TGFF) [3], Hybrid Latch-Flip-Flop (HLFF) [4], Sense Amplifier-based Flip-Flop (SAFF) [5], Modified SAFF [6], Differential Conditional-Capture Flip-Flop (DCCFF), and Single-ended Conditional-Capture Flip-Flop (SCCFF) [7]. TGFF has a fully static master–slave structure by cascading two identical pass-gate latches and provides a short clock-to-output latency. However, it has poor data-to-output latency because of positive setup time. It also requires two phases of clock that can cause a problem with data feedthrough when there is a skew between them. Moreover, it has a relatively large clock load. HLFF is actually a latch with a brief transparency period. The major advantage of the hybrid design is the soft-clock edge property which is desirable for robustness to clock skew. However, the major drawback is that the hold time has a positive value, mandating a detailed hold timing analysis to avoid a timing failure. SAFF incorporates a precharged sense amplifier and a Set-Reset (SR) latch to hold the data. In the SAFF, the SR latch is a NAND-based latch. The latency of the NAND-based SAFF [5] is longer than that of HLFF because one output is delayed by one gate delay from the other. This drawback was overcome by the modified SAFF having a symmetric slave latch [6] as shown in Fig 1(d). The modified SAFF also allows fully symmetrical output transitions. Conditional-capture flip-flops (DCCFF and SCCFF) achieve statistical power reduction by eliminating internal redundant transitions. They have negative setup time and thus provide small data-to-output latency [7]. For fair comparison, we compare the single-ended and differential flip-flops separately. TGFF, HLFF and SCCFF are single-ended flip-flops while SAFF and DCCFF are differential flip-flops.

3. Energy-recovery flip-flops

Fig. 2 shows the schematic diagram of energy recovery flip-flops, recently published in [8]. The first energy

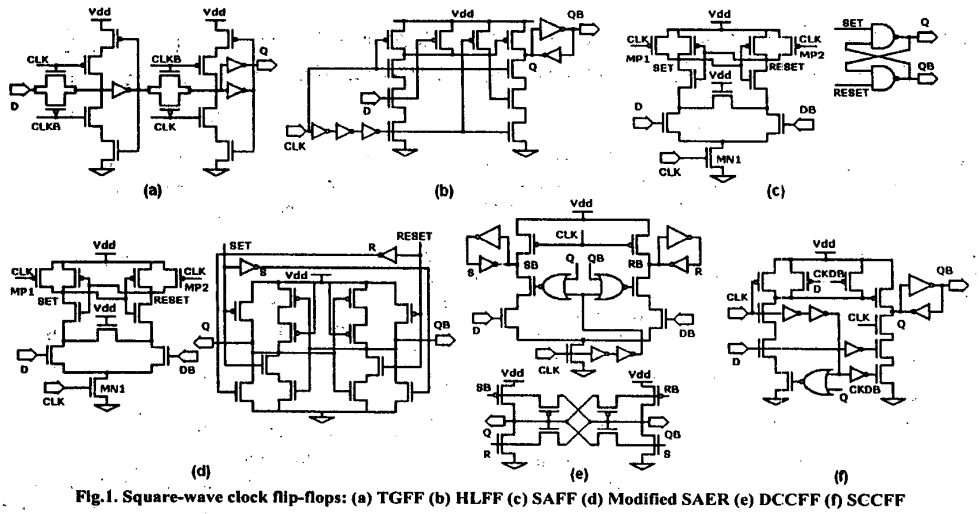

Fig.1. Square-wave clock flip-flops: (a) TGFF (b) HLFF (c) SAFF (d) Modified SAER (e) DCCFF (f) SCCFF

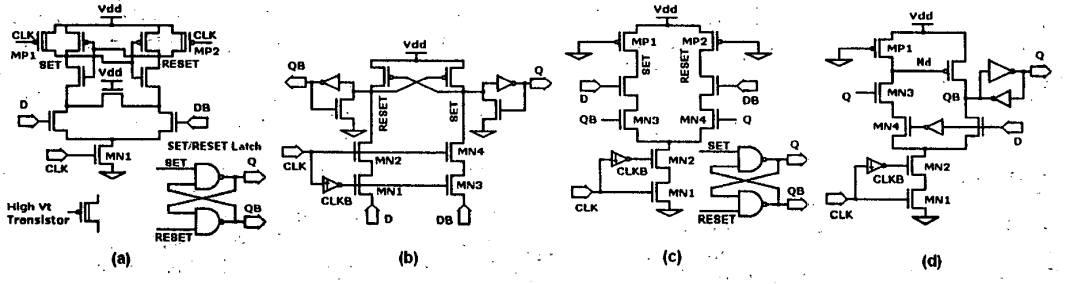

Fig. 2. Energy recovery flip-flops: (a) SAER (b) SDER (c) DCCER (d) SCCER [8]

recovery flip-flop, Sense Amplifier Energy Recovery (SAER) flip-flop [8], shown in Fig. 2(a), has the same structure as SAFF with NAND-based SR latch. This flip-flop is a dynamic flip-flop with precharge and evaluate phases of operation. It uses high threshold voltage (Vth) for PMOS precharging transistors to limit the short circuit current. For symmetric outputs, we also used the high-speed SR latch with cross-coupled circuit (shown in Fig. 3 [7]) instead of NAND SR latch. The latch captures each transition and holds the outputs until the next pull-down transition occurs on one of the precharge nodes. The cross-coupled circuit consisting of four weak transistors M5 through M8 is used for compensating the leakage and preserving the output data statically during the period in which the SR latch is opaque. The main problem of SAER is that it has substantial power consumption at low data switching activities due to redundant internal switching. Two approaches to address this problem are static operation and applying conditional capturing. Fig. 2(b) shows the Static Differential Energy Recovery (SDER) flip-flop [8]. The energy recovery clock is applied to a minimum-sized inverter skewed for fast high-to-low transition. In this flip-flop, when the state of the input data is the same as its state in the previous conduction phase,

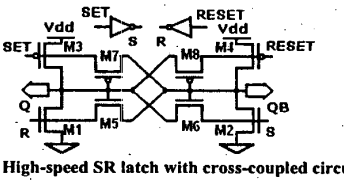

Fig. 3. High-speed SR latch with cross-coupled circuit.

there are no internal transitions. Therefore, power consumption is minimized for low data switching activities.

The second approach is to use conditional capturing. Fig. 2(c) shows the Differential Conditional-Capturing Energy Recovery (DCCER) flip-flop [8]. In DCCER flip-flop instead of using the clock for precharging, small pull-up PMOS transistors (MP1 and MP2) are used for charging the precharge nodes (SET and RESET). The DCCER flip-flop uses a NAND-based Set/Reset or the symmetric SR latch (Fig. 3) for the storage mechanism. The conditional capturing is implemented by using feedback from the output to control transistors MN3 and MN4 in the evaluation paths. Fig. 4 shows typical simulated waveforms of the DCCER flip-flop. Fig. 2(d) shows a Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop

[8]. SCCER is a single-ended version of the DCCER flip-flip. The transistor MN3, controlled by the output Q, provides conditional capturing.

4. Simulation results and comparisons

All the flip-flops were designed using the BPTM 0.18μm process technology [9] with a supply voltage of 1.8V. The designs were optimized for a clock frequency of 200MHz. A load capacitance of 30fF was used for all outputs. Transistor sizing was optimized using an iterative procedure with the objective of achieving high speed and low power (minimum PDP) for all square wave clock and energy recovery flip-flops.

Fig. 5 illustrates the timing definitions for energy recovery flip-flops with the sinusoidal clock [8]. Similar definition is used for square wave clock flip-flops. Delay is measured between 50% points of signal transitions.

Setup time is the time from when data becomes stable to the rising transition of the clock. Hold time is the time from the rising transition of the clock to the earliest time that data may change after being sampled. In all figures the term "NAND" was used to distinguish the flip-flop with NAND-based SR latch from the flip-flop with the symmetric SR latch (Fig. 3). Fig. 6(a), (b), and (c) show clock-to-output (CLK-Q) delay and data-to-output (D-Q) delay vs. setup time for differential energy recovery flip-flops, square wave clock flip-flops along with DCCER, and single-ended flip-flops along with SCCER, respectively. For fair comparison, we compare the single-ended and differential flip-flops separately. For any flip-flop, there is an optimum setup-time that results in a minimum D-Q delay. As shown in Fig. 6, the CLK-Q delay becomes independent of setup time for long setup times. We use this value of CLK-Q delay for comparisons of CLK-Q delay. SAER flip-flop shows the smallest CLK-Q delay and the SDER flip-flop has the shortest setup time among the differential flip-flops. For small setup times, it is apparent that DCCER and SCCER flip-flops have the best D-Q delays among energy recovery flip-flops. Therefore, we have shown the delay of these energy recovery flip-flops in comparison with the square-wave clock flip-flops in Fig. 6 (b) and (c). It is apparent from Fig. 6 (b) and (c) that DCCER and SCCER flip-flops exhibit better delay compared to the square wave clock flip-flops. Fig. 7(a) and (b) show power as a function of data switching activity for different flip-flops. The DCCER flip-flop has the lowest power consumption at all switching activities among all the differential flip-flops while SDER has the maximum power at high switching activities. The SCCER flip-flop shows less power consumption compared to the square-wave clock flip-flops at switching activities higher than 30% and TGFF shows the lowest power consumption at low switching activities. It is obvious that energy recovery flip-flops show approximately lower power consumption in all data switching activities. More simulations showed that DCCER and SCCER flip-flops have the lowest PDP at

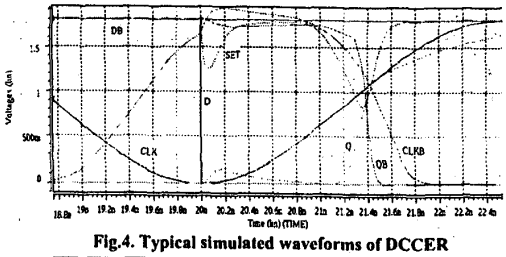

Fig.4. Typical simulated waveforms of DCCER

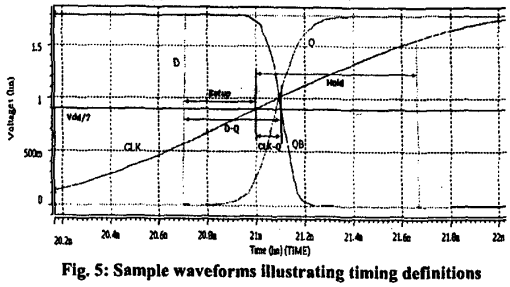

Fig. 5: Sample waveforms illustrating timing definitions

different frequencies and different supply voltages among the differential and single-ended flip-flops, respectively.

Table I summarizes the numerical results for differential and single-ended flip-flops. The DCCER flip-flop has the best D-Q delay, power, and PDP in differential energy-recovery flip-flops. DCCFF flip-flop has the best D-Q delay, power, and PDP in differential square-wave clock flip-flops. As compared to DCCFF, DCCER exhibits improvements of 14%, 43%, and 51% in delay, power, and PDP, respectively. The SCCER is the only single-ended energy recovery flip-flop. SCCER flip-flop exhibits 22% delay as compared with HLFF flip-flop, which has the best D-Q delay among single-ended square-wave clock flip-flops. The SCCER flip-flop exhibits 16% power reduction and 25% PDP reduction as compared with TGFF, which has the best power and PDP among single-ended square-wave clock flip-flops. Moreover, the energy recovery flip-flops have smaller area (transistor width and transistor count) in comparison to the square-wave clock flip-flops.

5. *Conclusions*

We presented an extensive power, delay, and area comparison between energy recovery and square-wave clock flip-flops. Based on our simulation results, the energy recovery flip-flops exhibit significant delay, power, and area improvements compared to the square-wave clock flip-flops. Therefore, our results show that energy-recovery flip-flops are not only beneficial for energy savings on the clock tree, but also for saving on the flip-flop power.

References

[1] S.D. Naffziger and G. Hammond, "The implementation of the next generation 64b ItaniumTM microprocessor," IEEE International Solid-State Circuits Conference, pp. 344-472, 2002.

[2] W. C. Athas, *et al.*, "Low-power digital systems based on adiabatic switching principles," IEEE Trans. VLSI Systems, vol. 2, no. 4, pp. 398-406, Dec. 1994.

[3] G. Gerosa *et al.*, "A 2.2 W 80 MHz superscalar RISC microprocessor," IEEE J. Solid-State Circuits, vol. 29, pp. 1440–1452, Dec. 1994.
[4] H. Partovi *et al.*, "Flow-through latch and edge-triggered flip-flop hybrid elements," in Int. Solid-State Circuits Conf.e, Dig. of Tech. Papers, Feb. 1996, pp. 138–139.
[5] M. Matsui *et al.*, "A 200 MHz 13mm 2-D DCT macrocell using sense amplifying pipeline flip-flop scheme," IEEE J. Solid-State Circuits, vol. 29, pp. 1482–1490, Dec. 1994.
[6] B. Nikolic, *et al.*, "Improved sense-amplifier-based flip-flop: design and measurements," IEEE Journal of Solid-State Circuits, vol. 35, pp. 876 -884, Jun 2000.
[7] B. S. Kong, *et al.*, "Conditional-capture flip-flop for statistical power reduction," IEEE Journal of Solid-State Circuits, vol. 36, pp. 1263 – 1271, Aug. 2001.
[8] M. Cooke, H. Mahmoodi-Meimand, and K. Roy, "Energy Recovery Clocking Scheme and Flip-Flops for Ultra Low-Energy Applications" International Symposium on Low Power Electronic Design, Aug. 2003
[9] Berkeley Predictive Technology Model, http://www-device.eecs.berkeley.edu/~ptm

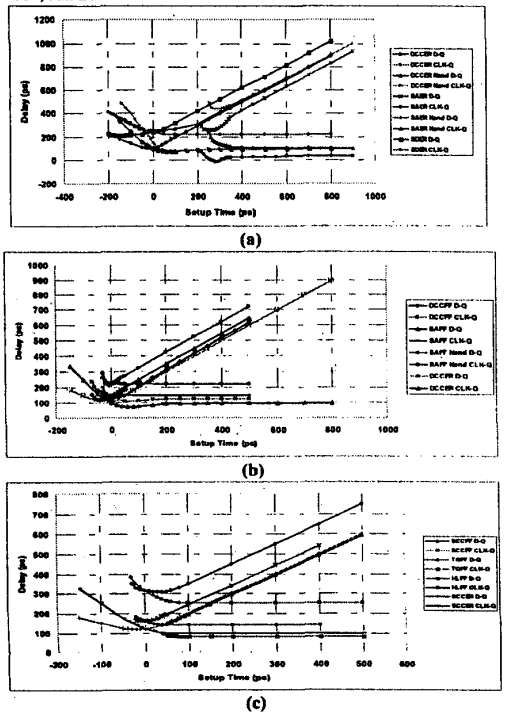

Fig. 6: Delay vs. setup time for (a) energy recovery flip-flops (b) differential square wave clock flip-flops along with DCCER (c) single-ended flip-flops square wave clock flip-flops along with SCCER

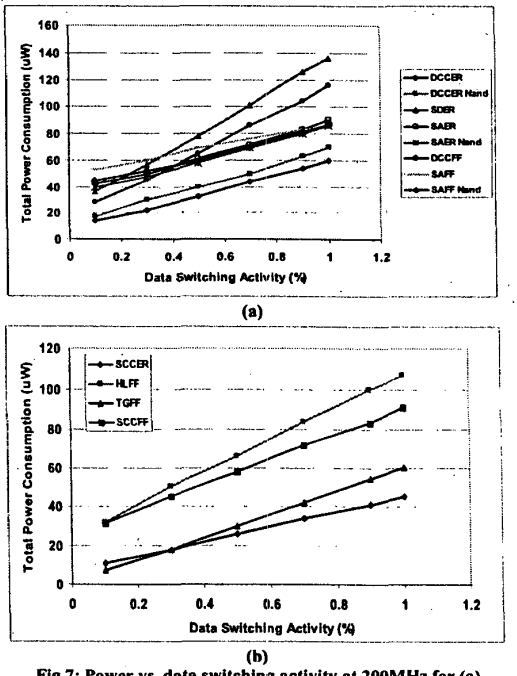

Fig.7: Power vs. data switching activity at 200MHz for (a) differential flip-flops (b) single-ended flip-flops

Table 1: Numerical results at 50% data switching activity with 200MHz clock (a) differential flip-flops (b) single ended flip-flops (square-wave flip-flops are shown in shaded rows)

(a)

	Min D-Q delay (pS)	Setup time (pS)	Hold time (pS)	CLK-Q delay (pS)	Power (μW)	PDP (fJ)	Norm. PDP	Transistor count	Total Transistor Width (μm)
SAFF NAND	213.7	-9.5	27.5	222.6	60.1	12.84	0.501	18	28.1
SAFF	140.4	-10.3	33.2	148.2	68.1	9.56	0.377	26	28.8
DCCFF	125.7	-25.2	34.2	124.6	56.8	7.14	0.279	35	47.0
DCCER	108.3	-11.9	41.7	73.6	32.3	3.50	0.136	22	22.8
DCCER NAND	226.1	12.5	61.2	101.4	78.1	17.66	0.682	18	22.5
SAER	260.3	262.7	52.6	30.2	62.5	16.27	0.635	22	27.6
SAER NAND	446.7	290.3	58.5	115.7	57.3	25.59	1	18	27.3
SDER	215.6	-72.3	271.7	221.3	78.9	17.01	0.664	14	45.8

(b)

TGFF	144.6	40.3	25.3	83.1	34.5	4.99	0.195	18	28.1
HLFF	162.1	-13.5	113.1	142.9	65.6	10.68	0.417	20	31.4
SCCFF	309.7	-17.3	21.5	252.6	56.9	17.62	0.688	26	34.9
SCCER	129.2	52.3	57.4	82.5	28.9	3.73	0.145	15	24.0