Efficiency of Adiabatic Logic for Low-Power, Low-Noise VLSI

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Abstract-In this paper, the efficiency of a fully adiabatic logic circuit is compared with its combinational and pipelined static CMOS counterparts. The performance of each circuit is studied in terms of the maximum frequency of operation, the minimum voltage of operation, the circuit energy consumption, and the switching noise generated by the circuit. An 8-bit carry look-ahead adder is designed using a 0.6-μm CMOS technology for all three logic styles. Based on the post-layout simulation results, the adiabatic adder exhibits energy savings of 76% to 87% and 87% to 90% compared to its combinational and pipelined static CMOS counterparts, respectively. It also exhibits a considerable reduction in switching noise, compared to its static CMOS counterparts.

I. INTRODUCTION

Demands for low power and low noise digital circuits have motivated VLSI designers to explore new approaches to the design of VLSI circuits. Energy-recovering (adiabatic) logic is a new promising approach, which has been originally developed for low power digital circuits [1-3]. Adiabatic circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors [4].

Another major advantage of adiabatic logic families is their best behavior for lower generation of switching noise, which is becoming one of the most important problems in current digital and especially in mixed mode integrated circuits. The traditional solution of employing on chip decoupling capacitors to combat the supply noise results in an unacceptable area increase [5]. Invoking adiabatic logic circuits will reduce the switching noise of digital circuits. The reason is that in these circuits, the switching occurs with the minimum voltage drop across devices and nodes voltages change slowly. To the best of our knowledge no report on the efficiency of the switching noise characteristic of the adiabatic logic circuits has been published in the literature.

In this paper, we present the results of comparison between an adiabatic logic circuit and its combinational and pipelined static CMOS counterparts, in terms of the maximum frequency of operation, the minimum voltage of operation, the energy consumption, and the switching noise generation of the circuit. The logic circuit is an 8-bit carry look-ahead adder (CLA) which has been implemented using all three logic styles. The adiabatic logic is based on Pass-transistor Adiabatic Logic (PAL) proposed in [1] and has a fully adiabatic operation. Although the study is performed for this type of adiabatic

logic, the results can be extended to other types of adiabatic logic. The structure of the paper is as follows. In Section II, an overview of PAL is given. The adder designs are described in Section III while the results are presented in Section IV. Finally, Section V contains the summary and conclusion of the paper.

II. PAL OVERVIEW

PAL is a dual-rail adiabatic logic with a relatively low gate complexity that operates with a two-phase power clock [1].

A. PAL Gates

A PAL gate consists of true and complementary pass-transistor NMOS functional blocks (f, /f), and a cross-coupled PMOS latch (MP1, MP2), as illustrated by the example of Fig. 1, which shows the implementation of an AND-OR gate: Q=A·B+C. The power is supplied through a sinusoidal power-clock (PC). When PC starts rising from low, input states make a conduction path from the power clock (PC) through one of the functional blocks to the corresponding output node and allow it to follow the power clock. The other node will be tri-state and kept close to 0V by its load capacitance. This in turn causes one of the PMOS transistors to conduct and charge the node that should go to one state, up to the peak of PC. The output state is valid at around the top of the power clock. The power clock will then ramp down toward zero, recovering the energy stored on the output node capacitance.

B. PAL Cascades
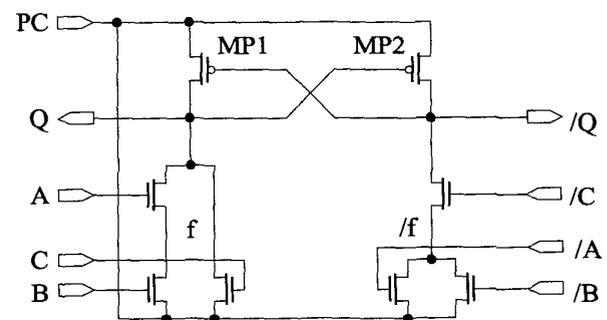
Cascade of logic gates is provided by alternate

Fig. 1. Implementation of Q=A·B+C in PAL

connection of their power clock ports to PC and its 180° phase shifted signal (/PC). Both PC and /PC can be obtained from an efficient LC oscillator and there will be no extra overhead for the generation of /PC. A cascade of four PAL inverters is shown in Fig. 2. All odd logic stages are supplied by the sinusoidal voltage PC, while all the even logic stages are supplied by /PC. The logic operation has only two phases: evaluate (E), when the power clock is ramping up, and discharge (D), when the power clock is ramping down. The E phase of an odd
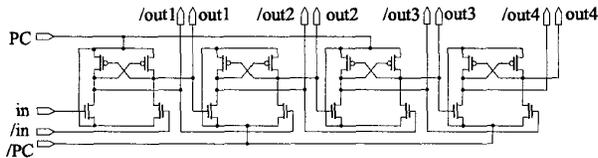

Fig. 2. A 4-stage cascade of PAL inverters

Fig. 3. Waveforms obtained from HSPICE simulations of a 4-stage pipeline of PAL inverters. (a) power clock (PC and /PC), (b) input of 1st stage, (c) output of 1st stage, (d) output of 2nd stage, (e) output of 3rd stage, and (f) output of 4th stage.

stage coincides with the D phase of an even stage and vice versa. Fig. 3 shows the timing of the signals in a PAL cascade obtained from the HSPICE simulations of this cascade at 10MHz with a 0.6-μm CMOS technology. The input signal was periodic sequence 01110111.... More information regarding the operation of PAL can be found in [1].

III. ADDER DESIGNS

For a fair comparison, all CLAs have the same logic architecture. The schematic diagram of the 8-bit CLA is shown in Fig. 4. The full custom layout of the adiabatic CLA consists of 445 transistors. All device sizes are minimum size in a 0.6-μm CMOS technology. The adiabatic adder is similar to a 6-stage pipelined adder with two phase clocking. It generates one output each cycle and has a latency of 3 cycles. Each primary output was connected to a 50fF load.

To compare the performance of this adiabatic circuit, we developed two non-adiabatic designs with static CMOS logic. The first design was a purely combinational CLA while the second one was a pipelined version of the fully combinational design. In order to have the same architecture as adiabatic CLA circuit we implemented the pipelined CLA in a 6-stage architecture with two phase clocking, which has a latency of 3 cycles, equal to the
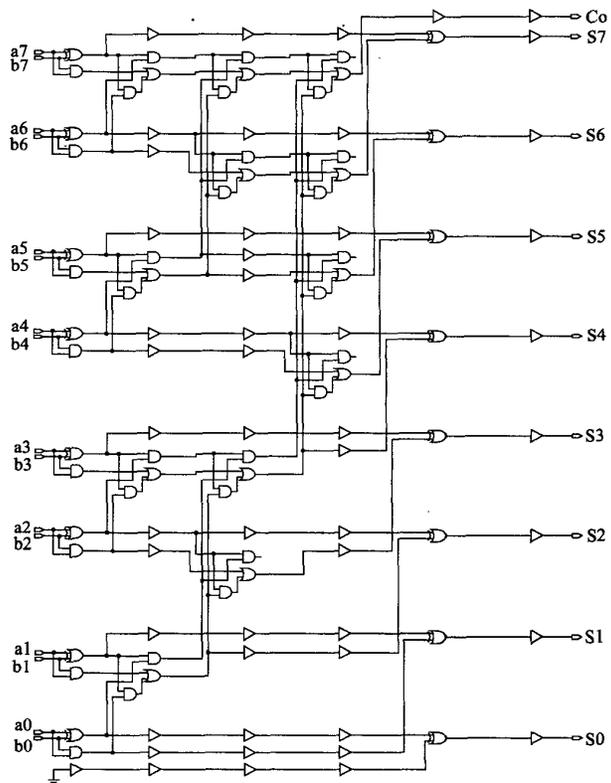

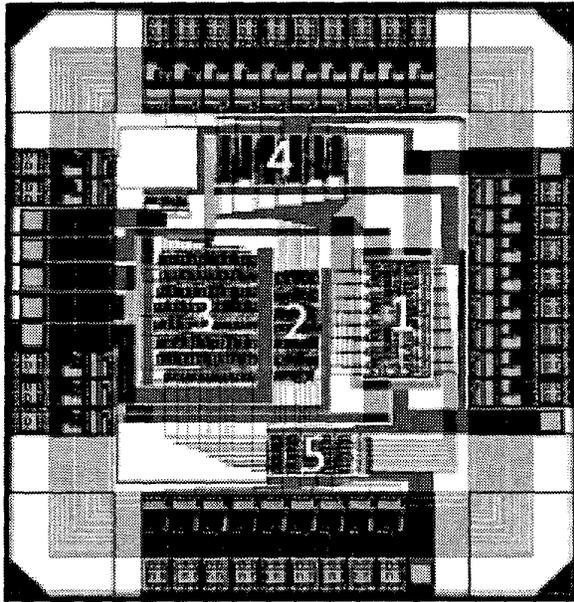Fig. 4. Schematic diagram of 8-bit CLA

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Fig. 5. Layout of the test chip: (1) Adiabatic CLA (2) Combinational CLA (3) Pipelined CLA (4) Input demultiplexer (5) Output multiplexer

latency of the adiabatic CLA circuit. The layouts of the two designs were generated using standard cells and the LEDIT placement and routing tool. Standard cells were optimized for low power and high speed. The combinational and pipelined CLA consist of 704 and 3596 transistors, respectively. We have integrated these three layouts in a test chip, which has been submitted for fabrication. To limit the pin count of the experimental chip to 40 pins, input demultiplexers and output multiplexers have also been integrated in the test chip. To facilitate the net power measurement of the circuits, the power lines of the CLA blocks and other parts of the chip are separated. Fig. 5 shows the layout of the test chip, which has a die area of $5mm^2$.

IV. SIMULATION RESULTS

In this section, we present the results of the HSPICE simulations for the adders. The circuits were simulated with the netlists extracted from the layouts. The simulations computed the dissipation of the gates and internal clock lines but did not include the energy consumed on the external clock distribution network or the power clock generator. At each frequency, the results obtained for the minimum supply voltage that ensured correct function of each circuit. We also applied the worst case input pattern to the adders that would cause the maximum rate of events on the circuit nodes and, hence, the maximum switching noise and power consumption. In contrast to the static CMOS logic, the power consumption of the adiabatic circuit is independent of the data

propagated through it, since the adiabatic logic is fully differential.

A. Energy Consumption Results

Fig. 6 shows the energy consumption per cycle of the adders when operating at 10MHz, 50MHz, 100MHz, 150MHz, and 200MHz. The minimum supply voltage for each design is shown next to its data point. As expected, the pipelined design has the lowest minimum operating voltage and the adiabatic design has the highest one. However, the adiabatic design has the least energy consumption among the designs. Compared to the combinational adder, the adiabatic adder exhibits energy savings of 87% at 10MHz and 76% at 100MHz. In comparison with the pipelined adder, the adiabatic adder exhibits energy savings of 87% at 10MHz and 90% at 100MHz.

Fig. 7 gives the same information while the operating voltage is constant 3.3V over all frequencies. As expected the energy consumption per cycle of the static CMOS implementations do not vary with the operating frequency. Although, the energy consumption of the adiabatic CLA increases with the frequency, however, it has the lowest energy dissipation. In comparison to the combinational CLA, the adiabatic adder exhibits energy savings of 94% at 10MHz decreasing to 84% at 100MHz while in comparison to the pipelined CLA, the adiabatic adder exhibits energy savings of 99% at 10MHz decreasing to 96% at 100MHz. The adiabatic design fails to function above 100MHz, due to the short duration of the PAL evaluation phase. The adiabatic logic is more efficient for applications where the speed of operation is not very critical.

Fig. 8 gives the overall energy profiles of the adders at 10MHz while operating at their minimum supply voltage. It shows the energy recycling phenomenon of the adiabatic logic. Energy consumption of the combinational adder occurs at the times of the input transitions and energy consumption of the pipelined adder occurs at the active edges of the clocks.
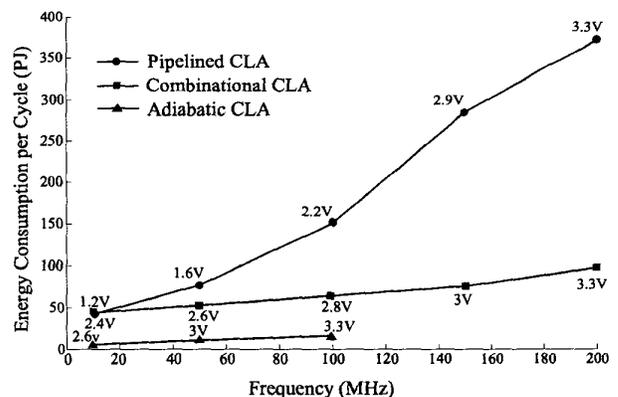

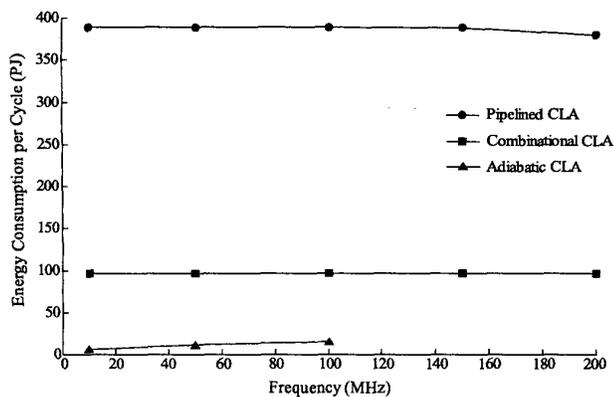Fig. 6. Energy consumption vs. frequency

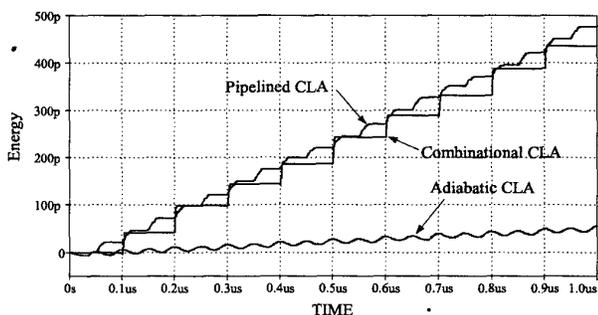Fig. 7. Energy consumption vs. frequency at constant 3.3V supply voltage
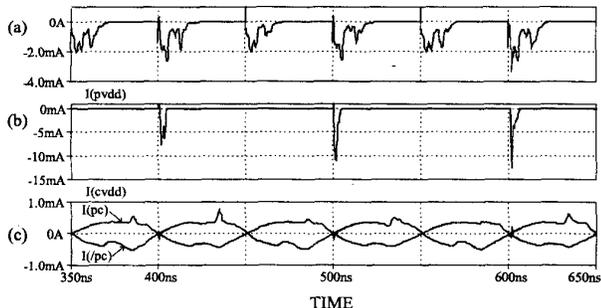

Fig. 8. Energy profiles

Fig. 9. Switching current waveforms: (a) Pipelined CLA (b) Combinational CLA (c) Adiabatic CLA

B. Switching Noise Generation Results

Power supply switching noise is composed of resistive (IR) and inductive (LdI/dt) noise [6]. Here I is the supply current while L and R are the effective supply inductance and resistance, respectively. When a number of devices switch at the same time, the cumulative transient current (I) and the slew rate (dI/dt) can be very large. The best logic from this aspect is the one that causes the minimum current spike (I) and slew rate (dI/dt) on the supply lines. There are two specific characteristics in adiabatic circuits that cause them to have the best behavior for the lowest switching noise generation. First, in the adiabatic circuits, switchings occur with the minimum voltage drop across

devices. Second, both signals and power supplies change slowly. Thus, steep spikes can be effectively removed from the supply current resulting in a considerable decrease in switching noise.

Fig. 9 shows the switching current waveforms obtained for the CLAs when operating with their minimum supply voltage at 10MHz. The pipelined CLA has abrupt total switching currents at the active edges of the clocks. The maximum amplitude is 3.4mA with many peaks and valleys. The combinational CLA has abrupt switching currents at the input transitions with the maximum amplitude of 12.6mA. The switching current of the adiabatic CLA is much more regular and sinusoidal with maximum amplitude of 0.7mA. The maximum current slopes for the pipelined, combinational, and adiabatic designs are 47A/µs, 47A/µs, and 0.3A/µs, respectively. This means that the adiabatic design exhibits two orders of magnitude reduction in switching noise, compared to the static CMOS designs, assuming the same power supply effective inductance for all the designs.

V. SUMMARY AND CONCLUSION

In this paper, an adiabatic logic style was compared with the combinational and pipelined static CMOS logic style by designing an 8-bit carry look-ahead adder using all three methods with a 0.6-µm technology. Based on the post-layout simulation results, the adiabatic CLA exhibits energy savings of 76% to 90% and two orders of magnitude reduction in switching noise, compared to its static CMOS counterparts. At each operating frequency, the adiabatic design has the highest minimum supply voltage. The maximum operating frequency of the adiabatic design is about 2 times less than that of the static CMOS designs. In conclusion, while the adiabatic logic family studied here exhibits considerable improvements in terms of energy savings and switching noise characteristics, it has the disadvantages of higher supply voltage and lower speed of operation.

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