Ultra Low Power Full Adder Topologies

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Abstract: In this paper several low power full adder topologies are presented. The main idea of these circuits is based on the sense energy recovery full adder (SERF) design and the GDI (Gate diffusion input) technique. These subthreshold circuits are employed for ultra low power applications. While the proposed circuits have some area overhead that is negligible, they have at least 62% less power dissipation when compared with existing designs. In this paper, 65nm standard models are used for simulations.

Keywords: GDI, SERF, Full adder, Subthreshold

I. INTRODUCTION

With the rapid development of portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts [1]-[4]. The role of power dissipation in VLSI systems is pervasive. For high performance design, power dissipation can be the limiting factor to clock speed and circuit density because of the inability to get power to circuits or to remove the heat that they generate. For portable information systems, power dissipation has a direct bearing on size, weight, cost, and battery life. Consequently, power dissipation is becoming widely recognized as a top-priority issue for VLSI circuit design. The challenge facing the VLSI designer is to find and effectively apply circuit techniques that can balance the needs for performance with those of power dissipation [5]. Therefore ultra low power circuits design becomes the major candidates for portable applications. One common technique for reducing power is power supply scaling. For CMOS circuits the cost of lower supply voltage is lower performance. Scaling the threshold voltage can limit this performance loss somewhat but results in increased leakages [6]. Other techniques used in low power design include clock gating and dynamic voltage/frequency scaling [7], [8].

Subthreshold circuit design involves scaling the supply voltage below the threshold voltage, where load capacitances are charged/discharged by subthreshold leakage currents. Leakage currents are orders of magnitude lower than drain currents in the strong inversion regime, so there is a significant limit on the maximum performance of subthreshold circuits. Therefore, traditionally, subthreshold circuits have been used for applications which require ultra-low power dissipation, with low-to-moderate circuit performance [9].

The 1-Bit Full adder design is one of the most critical components of a processor that determines its throughput, as it is used in ALU, the floating point unit, and address generation in case of cache or memory accesses [9]. A variety of full adders have been reported in [10]-[13]. One of the most well known full adders is the standard CMOS full adder that uses 28 transistors as shown in Fig.1. In [10] the sense energy recovery full adder (SERF) is presented. The topology of this circuit is shown in Fig.2 which requires only 10 transistors to implement a full adder. In [12] different full adder topologies with a low number of transistors are presented. In the next section the drawbacks of these SERF based circuits are described. In this paper different topologies for full adder based on GDI technique are presented. Moreover, several circuit topologies based on SERF full adder are presented for ultra low supply voltage applications. The multi threshold technique is used to improve the operation of the SERF full adder design.

II. PREVIOUS WORKS:

SERF design uses only 10 transistors to implement a full adder. This circuit operates well at higher supply voltages, but if the supply voltage is scaled to voltages lower than 0.3V, this circuit fails to work. Table I describes the behavior of this circuit for different inputs.

The rest of the paper is organized as follows: In section II, we briefly describe the previous works on full adder design. Section III presents new full adders and some simulations. In Section IV, the simulation results are presented and discussed. Section V is the conclusion.

Table I Truth table of SERF full adder design

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Cin</th>
<th>Sum</th>
<th>Cout</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>VDD-Vth</td>
<td>~0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Vtp</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>~Vtp</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Power consuming (is shown in Fig.3)</td>
<td>VDD-2Vth (in Fig.1)</td>
</tr>
</tbody>
</table>

In A=1, B=1, and Cin=0, the equivalent circuit for SUM signal is

\[ \text{Power consumption}= VDD-2Vth \] 

when Cin=0 and Cout will be equal to VDD-2Vth and the Sum signal is going to zero driven by a MOS transistor with its gate connected to VDD-Vth. When Cin=1, Cout is connected to VDD (may be lower) and the SUM signal will go to VDD-Vth. Another problem with this design is when the floating node is connected to 0 (A=0, B=1 or A=1, B=0). When Cin is “1”, Cout is charged to Vdd, but when Cin=0, Cout must be discharged to ground using a MOS pass transistor that cannot fully discharge the output. In this case, Cout is discharged to Vpp which is higher than Vth. This problem is intensified if the circuit was at subthreshold voltage. If A is at logic “1”, some current leaks to the Cout node which makes Cout to increase even more than Vpp in some cases depending on the sizing of the pass transistors. In this case the Sum value is dependent on the Cin state, for instance, if Cin is “1”, the Sum output is going to Vdd-Vth which is a problem in subthreshold region.

The most important problem with SERF full adder is in the case when A=1, B=1 and Cin=0. In this case as mentioned before the output signal reaches VDD. Simulation results show that at VDD=0.3V, the output signal is rising only to 0.1V which is not high enough to change the state of the next stage. To eliminate these problems a new topology must be introduced. This limitation also causes a constraint for lowering the supply voltage. For instance, to have a correct output for SUM it seems that the supply voltage cannot be lowered more than Vdd/2+2Vtn indicating that the supply voltage must be higher than VDD/2+0.28v in a 65nm CMOS technology. However this limit depends on the circuit design topology and also the sizing and the device types that are employed. To mitigate this problem, the gates of PT for Cout must be connected to Vdd during the challenging state (A=B=1, Cin=0). Then the supply voltage may be reduced to as low as Vdd/2-Vth which is estimated to be VDD/2-0.14. For example when VDD=0.3, in worst case Cout will then be Vdd-Vth=0.16V, which can be used as a high logic. In addition the NMOS pass transistor may be upsized to further lower the supply voltage. It seems to be possible to lower supply voltage to 0.25V.

In A=1, B=1, and Cin=0, the equivalent circuit for SUM signal is shown in Fig.3. As it can be seen, we cannot decide exactly the state
of the output, because, in this case, two PMOS devices and also the NMOS transistors are ON, then the output state is roughly dependent on the transistor. As a consequence the circuit fails to evaluate correctly in some cases. Now, we investigate the other SERF full adders' behavior in Fig.4 for input vector ABCin="11X". As it can be seen in Fig.4, this topology consumes much power with the input vector ABCin="110". At ultra low supply voltage the probability of failure is higher than when operating at higher supply voltages. Fig.5 shows the behavior of the topology in Fig.2 (c) during these two input vectors (ABCin="110" and ABCin="111").

In this topology the behavior of the circuit is improved compared with Fig.2 (b), so we can reduce the supply voltage as much as Vth compared to the circuit shown in Fig2(b). In the topology of Fig.2(d), there is the same problem for the SUM output signal. Fig.6 describes the behavior of this circuit. In Fig.6, if we add a circuitry, to connect the gates of the pass transistors to VDD instead VDD-Vth, the power dissipating path is removed due to the completely turned-off PMOS transistors, and also the output is connected to VDD-Vth instead of VDD-2Vth.

There are two solutions to improve the operation of SERF circuit. The first one is connecting the output of XNOR gate (first stage) to VDD instead of VDD-Vth (when the output of XNOR gate is high) and also powering Cout to be connected to VDD instead of VDD-Vth. The multiplexer-based SERF adder circuit is presented in [11]. In this circuit which is shown in Fig.7, all parts are implemented using a multiplexer. Although this circuit consumes less power than previous SERF topologies, it has some serious problems at lower supply voltages. Table.2 shows the truth table of this circuit.

In this section we analyze the Gate-Diffusion Input (GDI) full adder design that is proposed in [14]. The GDI technique is proposed by Morgenshtein et. al. in [4]. This technique reduces the power dissipation and also makes the circuit smaller. The advantage of GDI technique two-transistor implementation of complex logic functions, and in-cell swing restoration under certain operating conditions, are unique within existing low-power design techniques [4]. Fig.8 shows the operation of GDI technique and also implementation of a XOR gate using this technique. As it can be seen most logic functions required can be implemented using a small number of devices.

To implement a XNOR gate using GDI, the places for applying B and B can be changed. The problem with GDI-based adder is the same as for SERF adder. Fig.9 shows four topologies of GDI-based full adder. We analyze these full adders with different inputs. Table.3 shows the results for these full adders.

These GDI-based full adders work better than SERF in most cases, but there are some limitations for them. When the input vector is ABCin="001", suppose that the circuit is working with VDD=0.3V and the threshold voltage for PMOS and NMOS circuit are -0.15 and 0.14 respectively. In this case, Fig.10, illustrates the problem which is even more degradation at lower supply voltages for the circuit from Fig.9. (c). The SUM signal value is not stable, because of insistent power dissipation and contention between NMOS and PMOS to determine the X node state. Also in Fig.9(a), there are problems with discharging the SUM node to zero. The SUM output is discharged only to 2Vth which is high enough to be assumed as ‘1’. However, this circuit dissipates less power than SERF full adders. We can modify the SERF full adder to work at lower supply voltages and alleviate the problem with these special input vectors for the GDI-based adder design. For the GDI full adder, we can reduce the supply voltage lower than supply voltage for SERF circuit.

Table 2. Truth table of MUX-based SERF

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Cin</th>
<th>Sum</th>
<th>Cout</th>
</tr>
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<tbody>
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<td>0</td>
<td>Vth</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Vdd-Vth</td>
<td>Vth</td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Vdd-Vth</td>
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<td>Vdd</td>
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<td>Vdd-Vth</td>
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<td>1</td>
<td>1</td>
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<td>Vdd-Vth</td>
<td>Vdd</td>
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Fig. 12. This proposed circuit is shown in Fig. 13. This circuit enables the design using a compound of the techniques proposed in Fig. 11 and another idea that significantly improves the operation of the SERF uses one transistor more than the SERF full adder. Moreover, in the state when ABCin = “111”, the Cout is connected to VDD, and as a result, Sum is charged to VDD-Vth and the Cout is connected to VDD. The technique for Fig. 11 is used to improve the functionality of this circuit at lower supply voltages. The main drawback with the GDI full adder is when both X and Y are in logic low (AB = “00”). As it can be seen the main problem is with logic low (AB = “00”). As it can be seen the main problem is with the output of first stage XNOR gate in the GDI full adder. If we add a circuit to lower the output of first stage to logic zero instead of Vtp, there is no problem for this circuit anymore. Also, the original circuit dissipates much power during this state which is now reduced. The proposed GDI full adder is shown in Fig. 14. The added circuit is shown in bold lines in Fig. 14. When y and x signals are in logic low, this turns on the added NMOS transistor and helps to discharge F node voltage to zero. So this would alleviate the problem with this circuit described in Fig. 10. Fig. 15 shows the effect on the proposed GDI full adder output waveforms. We can add another transistor to the GDI full adder that is shown in Fig. 16. In this topology, NMOS transistor M2 is added to connect the SUM output signal to ground when G node voltage is high. This added NMOS transistor M2 enables this circuit to work in lower supply voltages.

Another proposed idea is as follows: We use a different configuration for the Cout signal and a Mux to produce the SUM signal of the output of XNOR gate. This topology is shown in Fig. 12. For this circuit, Table 4 shows that the logic levels of Cout are improved and the consuming path in SERF is mitigated. However this circuit uses one transistor more than the GDI full adder.

Another idea that significantly improves the operation of the SERF design is using a compound of the techniques proposed in Fig. 11 and Fig. 12. This proposed circuit is shown in Fig. 13. This circuit enables even more scaling of the supply voltage lower than Vtn+Vtp which is estimated to be 0.3V. Furthermore, we may use the precise sizing to enable the circuit to work in lower supply voltages. This circuit shows much better functionality compared with other SERF adder topologies. In this circuit, when A=1, B=1, Cin =0, there are no problems; because the F node is connected to “1”, which eliminates the power consuming path in Fig. 4. Because the gates of the pass transistors are connected to VDD, the PMOS transistor is off. Moreover, in the state when ABCin = “111”, the F node is connected to VDD, and as a result, Sum is charged to Vdd-Vth and the Cout is connected to VDD.

Another circuit that is proposed is a GDI based full adder design. The technique for Fig. 11 is used to improve the functionality of this circuit at lower supply voltages. The main drawback with the GDI full adder is when both X and Y are in logic low (AB = “00”). As it can be seen the main problem is with logic low (AB = “00”). As it can be seen the main problem is with the output of first stage XNOR gate in the GDI full adder. If we add a circuit to lower the output of first stage to logic zero instead of Vtp, there is no problem for this circuit anymore. Also, the original circuit dissipates much power during this state which is now reduced. The proposed GDI full adder is shown in Fig. 14. The added circuit is shown in bold lines in Fig. 14. When y and x signals are in logic low, this turns on the added NMOS transistor and helps to discharge F node voltage to zero. So this would alleviate the problem with this circuit described in Fig. 10. Fig. 15 shows the effect on the proposed GDI full adder output waveforms. We can add another transistor to the GDI full adder that is shown in Fig. 16. In this topology, NMOS transistor M2 is added to connect the SUM output signal to ground when G node voltage is high. This added NMOS transistor M2 enables this circuit to work in lower supply voltages.

IV. SIMULATIONS AND RESULTS:

We simulated FA circuits for different ranges of frequencies from 100 KHz to 10 MHz to find out which circuit performs well. We use the 65nm CMOS standard models. Also we simulated these circuits to find the lowest supply voltages that these circuits are able to work without failure. The results for all full adders in this paper are tabulated in Table 5 to show which full adder is best suited for operation in ultra low supply voltage applications. For SERF full adder, the most important drawback is its limitation on supply voltage scaling that which cannot be reduced below 2Vtn+Vtp. This problem is more challenging in corners especially in SS corner (Slow NMOS, Slow PMOS).

The supply voltage where SERF outputs are satisfactory is higher than 0.5V with high sized devices. The simulation results for different full adder circuits are shown in Table 5. As it can be seen in Table 5, the power consumption of SERF (Fig. 13) full adder is lower than other circuits. The supply voltage for this design is limited to voltages higher than 0.3V. For these designs we can use the lower supply voltages in some cases, but we have to use high sized devices that increase the area significantly. To find the minimum supply voltages for full adder designs, different inputs were applied at different frequency. We considered the functionality of these circuits in different operating conditions. For instance, as it is shown in Fig. 15, the dotted region shows the failure in SUM signal for GDI full adder at 0.3V supply voltage. In this case, for input vector BCin = “000”, SUM should be at zero logic. But it is discharged just to 0.16V, which can be assumed as high voltage causing a failure in circuit. As Table 5 shows, for proposed full adder topologies, power consumption is decreased significantly compared to conventional SERF and GDI full adder counterparts. The main reason of lower power consumption is using the lower supply voltages that cause reduction in dynamic power (quadratical) and also subthreshold power consumption (exponential). Table 6 shows the results for delay comparison for proposed circuits compared to other topologies in literature. As it’s shown, the proposed full adders improve the PDP in some cases by 2X times. For new GDI full adder designs, in proposed circuits, the PDP is improved compared to conventional GDI full adder circuit [4].
V. CONCLUSIONS

In this paper new full adder circuits are proposed to decrease the power consumption. According to transistor level simulations, the power consumption is decreased with at least 62% for the SERF design and 86% for the GDI full adder design. The cost is a small area overhead; the proposed circuits have a small area overhead up to 11% compared with SERF and GDI full adders. Also the GDI technique showed that this logic can be suitable for ultra low power applications.

REFERENCES: